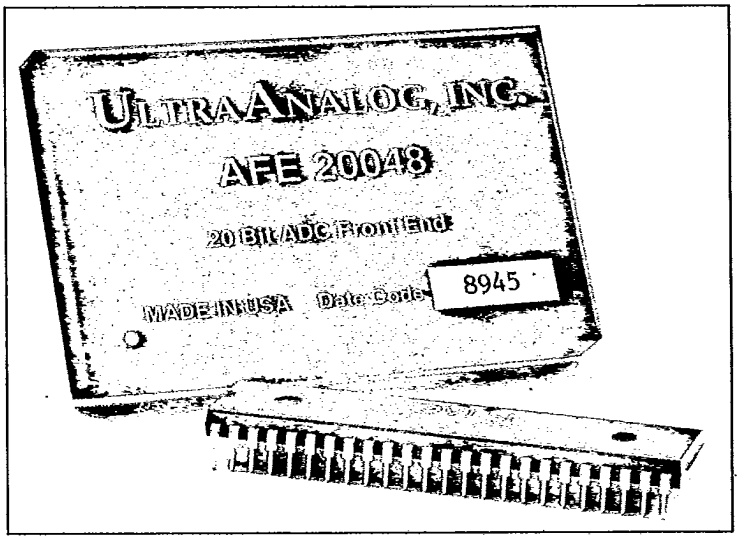

ULTRAANALOG, INC.
Advancing the Analog Art.

T-51-10-90

ADC 20048

20 Bit Audio ADC

Features

- 20-Bit Resolution
- 108dB Dynamic Range
- 128X Oversampling Rate
- Anti-Aliasing Filters Not Required
- <0.2LSB Diff. Linearity
- Pin-selectable 44.1 or 48kHz Output Data Rates
- Flat Frequency Response to within ±0.05dB
- Pin-selectable ±3V and ±5V Input Ranges

Applications

- Digital Audio Workstations
- Digital Mixing Consoles
- Digital Audio Routing Switchers
- Disk-based Recording
- Microphone Digitizing
- Upgrade 16-Bit Digital Audio Systems
- Sonar
- Analytical Instruments
- MRI Imaging

Description

The **UltraAnalog ADC 20048** advances the technology in digital audio converters by providing a complete 20-bit Analog-to-Digital Converter in a 2" x 3" shielded module and companion single 48-pin DIP. The **ADC 20048** architecture features a 128X oversampling, noise-shaping algorithm that eliminates the need for anti-aliasing filters and their associated noise, phase error, distortion and expense. The patented* data conversion algorithm, originally developed by dbx and refined by **UltraAnalog**, provides **108dB dynamic range**, passband **frequency response** flat to within **±0.05dB**, **-96dB THD and Noise**, and **no differential nonlinearity error** or **harmonic distortion** for low-amplitude signals.

The **ADC 20048** provides significant improvements in both performance and implementation over the original dbx versions of this ADC architecture. First, the ADC is complete within the **Analog Front-End** (**AFE 20048**) module and companion (**D20C10**) **Decimator** Filter DIP, requiring only power supply voltages, analog input and master clock signals to operate. All critical analog circuits are packaged within the **AFE** using double-sided, surface-mount technology which provides a highly reliable and economical converter. All of the necessary trimming and alignment, as well as adjustments for offset and distortion null, are done at the factory, using highly advanced, automated testing methods, which correct for all sources of non-linearity error. An internal timing generator provides high immunity to power supply noise which can cause clock jitter. Flat passband frequency response to ±0.05dB is achieved at both 44.1 and 48kHz sampling rates. At sampling rates other than 44.1kHz or 48kHz, the passband flatness degrades by ±0.025dB/%. Further, these rates are pin-selectable for ease of system configuration. Finally a differential input with pin-selectable ±3V or ±5V input ranges is provided.

* U.S. patent # 4,588,979

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Specifications

ANALOG INPUT

Input Voltage Ranges:	±3V, ±5V
Input Impedance:	Refer to Figure 1
Type:	Refer to Figure 1
CMRR:	60dB min.; dc-20kHz
Offset:	±5mV, max.
Offset Drift:	4 LSBs/°C, typ.; 20 LSBs/°C, max.
Gain:	±0.02dB, typ.; ±0.05dB, max.
Gain Drift:	±3ppm/°C, max.

DIGITAL INPUTS

Logic "0":	0V, min.; 1.5V, max.
Logic "1":	3.5V, min.; 5.0V, max.
Input Capacitance:	10pF, max.
Sampling Rate Clock Input:	40kHz, min.; 54kHz, max.
Master Clock Input:	256 x output data rate; 12.288MHz, nominal, for 48kHz data rate;
Output Enable:	Active low, i.e. Logic "0"
Format:	Logic "0"=2's complement; Logic "1"= offset binary

DIGITAL OUTPUTS[see Note 3]

Logic "0":	0.1V, max.at <1µA; -2.9mA output current
Logic "1":	4.9V, min. at <1µA; +2.9mA output current
Parallel Output Data:	20-bit parallel word
Serial Data Out:	Serial data bit stream; 20-bit word, 32-bit field
Bit Clock Out:	Bit clock for serial data
Word Clock Out:	Word clock for serial data

DYNAMIC PERFORMANCE

Differential Non-Linearity:	±0.2LSB
Integral Linearity:	<±0.001%
THD + Noise, typ.:	
20Hz-20kHz	
V_{OUT} = -2dB:	-96dB
V_{OUT} = -20dB:	-84dB
V_{OUT} = -40dB:	-66dB
V_{OUT} = -60dB:	-48dB
Dynamic Range	-108dB, typ. at 1kHz

FILTER CHARACTERISTICS

Frequency Response:	DC-20kHz, ±0.05dB
Passband	
44.1kHz Data Rate:	DC to 21.5kHz (-3dB)
48kHz Data Rate:	DC to 23.5kHz (-3dB)
Ripple:	±0.00087dB
Stopband	
44.1kHz Data Rate:	24.1kHz to 2.8MHz
48kHz Data Rate:	28kHz to 3.0MHz

POWER REQUIREMENTS [see Note 4]

Power Dissipation:	2.8 watts, typ.
+15.00 ±0.25V:	105mA, typ.
-15.00 ±0.25V:	40mA, typ.
+5.00 ±0.25V:	125mA, typ.

ENVIRONMENTAL

Operating Range:	0°C to +60°C
Storage Range:	-25°C to +85°C
Relative Humidity:	0 to 85%, non-condensing

MECHANICAL

AFE 20048

Dimensions:	2.0" x 3.0" x 0.4", max.
Material:	High thermal conductivity, black epoxy module
Shield:	Critical circuitry internally shielded

D20C10

Dimensions:	48-pin DIP
Material:	Plastic
Shield:	Not required

NOTES

1. All electrical specifications apply to the complete ADC, comprised of the AFE 20048 and D20C10 combination.
2. Dynamic performance characteristics are measured with either sampling frequency of 44.1 or 48kHz.
3. Refer to digital timing diagrams, ***Figures 2 and 3.***
4. The ±15V power supplies must be linearly regulated. The +5V supply must have less than $20mV_{p-p}$ switching spikes.
5. Specifications are subject to change without notice.

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AFE 20048/D20C10 Interconnections

Figure 1

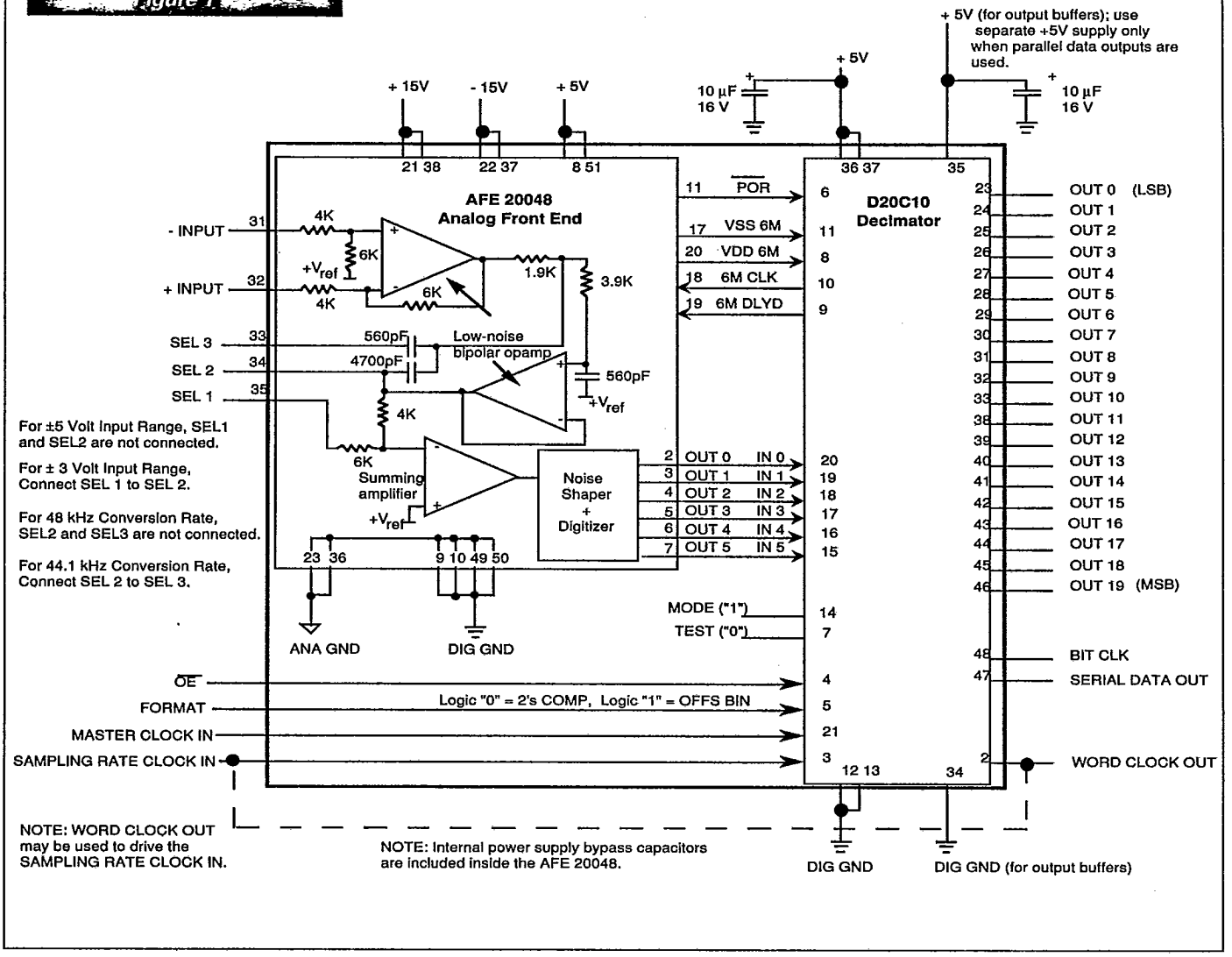

Figure 1, "AFE 20048/Decimator D20C10 Interconnection" shows the complete interconnection scheme to implement a 20-bit ADC converter using the **AFE 20048 Analog Front-End (AFE)** and **D20C10 Decimator** Filter IC (**Decimator**).

Power Supplies

The **AFE** requires three operating supply voltages, +15V ±0.25V, -15V ± 0.25V and +5V ±0.25V. The ±15V sources must be linearly regulated. Bypass capacitors are not required on the power supply lines, since they are included inside the **AFE**. The **Decimator** requires two separate +5V power supplies; one supply powers the **Decimator** itself, the second powers its parallel output latches. This arrangement isolates the **AFE** from any latch switching transients. The +5V supply connected to **Decimator** pins 36 and 37 may be the same one used to supply +5V power to the **AFE** module.

Digital I/O

The digital I/O of the **AFE** and **Decimator** are connected as shown in *Figure 1.* Lead lengths should be as short as possible, with extensive use of ground plane under both the **AFE** and the **Decimator**. Analog and digital grounds are internally tied together in the **AFE**. If desired, the WORD CLOCK OUT (pin 2) from the **Decimator** may be used to drive the SAMPLING RATE CLOCK INPUT (pin 3) of the **Decimator** directly; otherwise, a clock equal to the sampling rate, synchronized to the MASTER CLOCK INPUT per the timing diagrams in *Figure 2, "ADC 20048 Input Timing"* must be provided.

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Interconnections

I/O Format Options

Several pin-selectable options are provided relative to analog input full scale range, digital output data sampling rate and format. The input full scale range is normally ±5V. A ±3V input full scale range is selected by a jumper between **AFE** pin 35, SEL 1 and pin 34, SEL 2. Digital output data sampling rate is normally 48kHz. It can be set to 44.1kHz by a jumper between **AFE** pin 34, SEL 2 and pin 33, SEL 3. The digital output data format is set by logic level on the **Decimator** FORMAT pin (5). A logic low ("0") sets the output data to a 2's complement format, while a logic high ("1") sets the output data to offset binary.

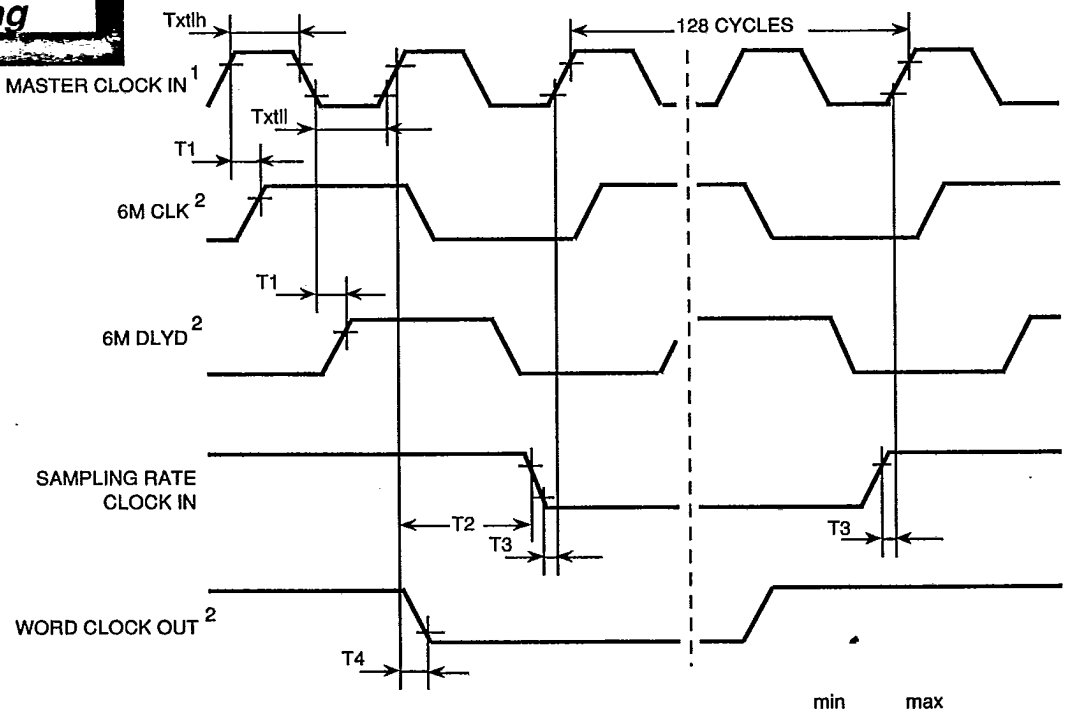
Sampling Rates and Required Clock Signals

Sampling rates other than 48kHz or 44.1kHz can be used, provided they are within the range of 40-54kHz. To use a sampling rate other than the two jumper-selectable rates, simply adjust the frequency of the master clock to be 256 x the desired sampling rate (e.g. for a 50.0kHz sampling rate, the master clock frequency would be 50.0kHz x 256 = 12.8MHz). For sampling rates from 40-46kHz, jumper between pin 34, SEL 2 and pin 33, SEL 3 on the **AFE**. For sampling rates from 46-54kHz, do not install any selection jumper. This optimizes the roll-off characteristics of the ADC 20048 to be as close to ideal as possible, although at sampling rates other than 44.1 or 48kHz, a small amount (<1.9dB) of roll-off or peaking at 20kHz will occur.

Options are also available relative to providing the sampling rate clock signals required by the **Decimator**, and for synchronizing multiple **ADC 20048** subsystems in multi-channel applications. The **Decimator** requires a precise sampling rate clock input, synchronized to the master 12MHz nominal clock. This sampling rate clock, which is equal to the desired output data rate, must be applied to pin 3, SAMPLING RATE CLOCK IN. Its frequency is MASTER CLOCK ÷256. The **Decimator** itself produces this signal at its WORD CLOCK OUT, pin 2. Unless there is a system-level reason to generate the sampling rate clock signal from the master 12MHz clock signal

ADC 20048 Input Timing

Figure 2



1. The MASTER CLOCK IN must be applied prior to power up to insure proper reset (POR) of the Decimator.

2. Shown for reference only.

	min	max	
Txtlh	35		ns
Txtll	35		ns
T1		40	ns
T2	0		ns
T3	10		ns
T4	0	40	ns

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elsewhere in the system, simply tying the WORD CLOCK OUT and SAMPLING RATE CLOCK IN pins together satisfies this signal requirement.

Serial Data Output

Serial output data is presented on the SERIAL DATA OUT pin (47), synchronized with the BIT CLOCK output on pin 48. The data is output as a 32-bit field, MSB first, with the last 12 bits set to zero. The data changes state on the high-to-low transition of the BIT CLOCK signal. The bit clock frequency is 32 times the sampling rate clock. Thus, for a 48kHz data sampling rate, the bit clock is 32x48kHz, or 1.536MHz. *Figure 3, "Serial Output Timing"* shows the timing relationship for serial data output from the **ADC 20048.**

Parallel Data Output

A logic low ("0") on pin 4, the OE (OUTPUT ENABLE) enables the tri-state output latches and presents the data on the output pins. The 20-bit parallel data outputs, pins 23 (LSB) to 33 and 38 to 46 (MSB), are disabled by a logic high ("1"). The timing relationships for parallel data output are shown in *Figure 3, "Parallel Output Timing"*.

Synchronizing Multiple ADC 20048's

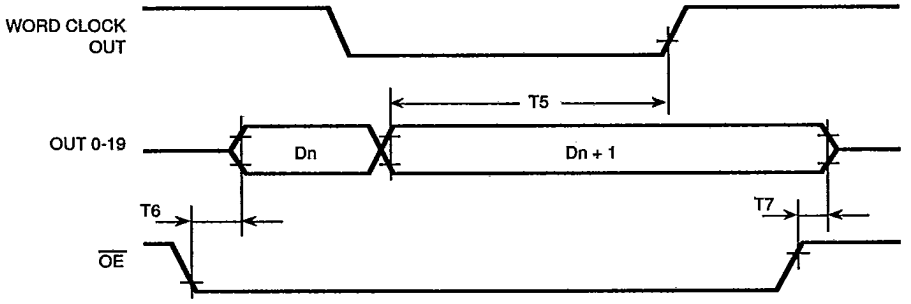
Multiple **AFE20048/D20C10** subsystems in a multi-channel system can be synchronized by connecting the master 12MHz clock signal to pin 21, MASTER CLOCK INPUT of each **Decimator**. If necessary, several non-inverting buffers in parallel can be used to increase the drive capability of the master clock signal for connecting to large numbers of **ADC 20048** without loading down the master clock source. The WORD CLOCK OUT from one of the **Decimators** must be connected to the SAMPLING RATE CLOCK IN on each of the **Decimators.**

Data Outputs

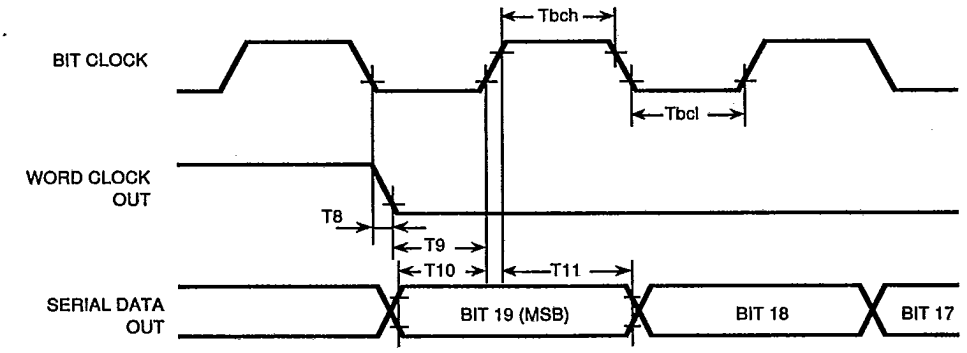
Output Data Timing

Figure 3

ADC20048 PARALLEL OUTPUT TIMING DIAGRAM



ADC20048 SERIAL OUTPUT TIMING DIAGRAM



	min	max	
T5	9000		ns
T6		45	ns
T7		65	ns
Tbch	280		ns
Tbcl	280		ns
T8	0	40	ns
T9	240		ns
T10	225		ns
T11	225		ns

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Principles of Operation

The **ADC 20048** consists of a differential amplifier, low-pass filter, summing amplifier, noise-shaping filter, 4-bit DAC and flash ADC, which feeds the **D20C10 Decimator**, all interconnected as shown in *Figure 4*.

AFE 20048 ANALOG FRONT-END

The analog signal is converted to a 4-bit digital approximation by the flash ADC at a 128X oversampling rate of 6.144MHz (128 x 48kHz data sampling rate). Since the conversion rate is significantly higher than the audio frequency range of interest, no aliased signals foldback into the audio band, and an anti-aliasing filter is not required ahead of the **ADC 20048**. However, relative to the 4-bit ADC, the quantization noise level within the DC-20kHz band would degrade the performance of the ADC considerably, if the noise were not randomized and its energy reduced by the noise-shaping filter directly ahead of the flash ADC. The low-pass filter is a second order peaked filter that compensates for a 1.9dB rolloff at 20kHz by the **Decimator**, such that the response within the 20-20kHz audio band is flat to within ±0.05dB.

The output of the flash ADC is applied simultaneously to the **Decimator** and the 4-bit DAC. The DAC output is subtracted from the analog input at the summing amplifier, resulting in an error signal which is integrated by the noise-shaping filter. The integration of the error signal guarantees that the average digital output of the ADC matches the input signal, within the accuracy of the DAC. With this summing amplifier—noise-shaping filter—flash ADC—4-bit DAC loop closed, the output of the ADC is a pattern of codes centered around the analog input value. With no input signal, the idle pattern of the ADC output is a random sequence of two or three contiguous codes, with energy slightly greater than the ADC quantization noise.

2's Complement, 0V Decimator Input

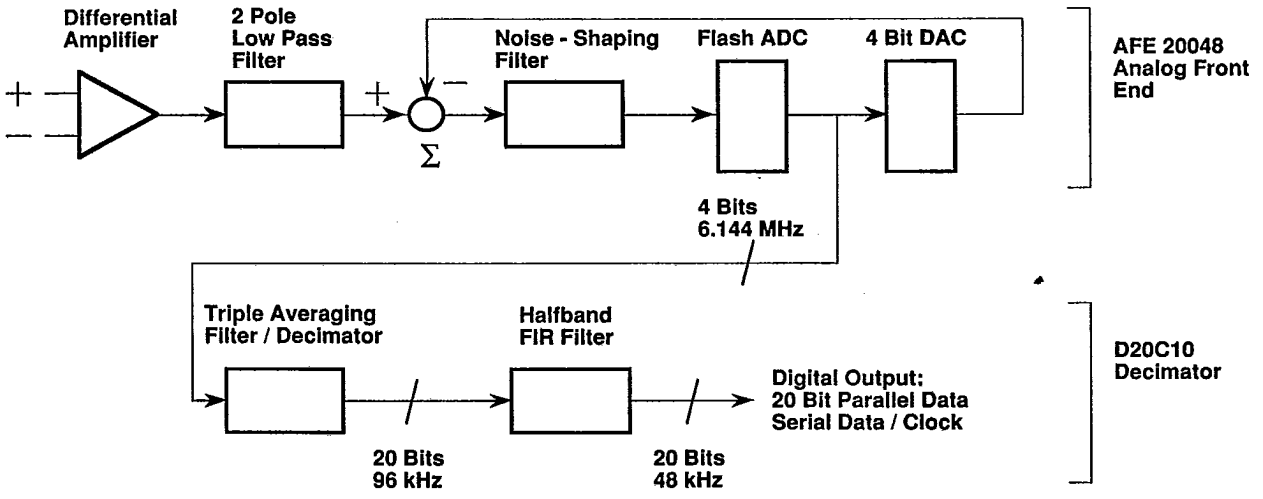
Figure 5

Input Voltage	4-Bit Front-end Output		2-LSB Fixed Output	2's Comp'lement 6-Bit Input	
-FS	0	1000	10	100010 =	-30
	1	1001	10	100110 =	-26
	2	1010	10	101010 =	-22
	3	1011	10	101110 =	-18
	4	1100	10	110010 =	-14
	5	1101	10	110110 =	-10
	6	1110	10	111010 =	-6
0V	7	1111	10	111110 =	-2
	8	0000	10	000010 =	2
	9	0001	10	000110 =	6
	10	0010	10	001010 =	10
	11	0011	10	001110 =	14
	12	0100	10	010010 =	18
	13	0101	10	010110 =	22
	14	0110	10	011010 =	26
+FS	15	0111	10	011110 =	30

The output of the flash ADC is a 4-bit word, while the input to the **Decimator** is six bits. The two LSB's of the six bits sent to the **Decimator** are hard-wired inside the **AFE** as a 1-0 combination. Given the 2's complement format of the input word to the **Decimator**, this has the following desired effect — with 0Volts input, which corresponds to mid-scale, the 4-bit output pattern of the ADC itself

Functional Block Diagram

Figure 4



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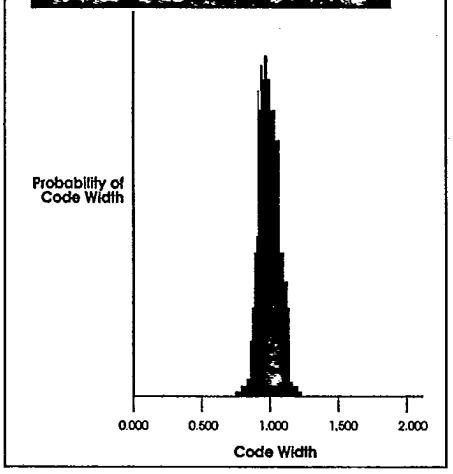
would produce equal probability of "7" or "8" codes, with a few "6's" and "9's" mixed in. With the 5th and 6th bits added in, at 1-0, respectively, the 2's complement words have an average value of zero, which produces zero, or half-scale in a binary mode. This is the desired output for a 0Volt input. (Please refer to *Figure 5.)*

D20C10 DECIMATOR

The **Decimator** accepts the 6-bit 2's complement data from the **AFE 20048** and performs three filtering actions. First it removes the out of band noise and increases the resolution to 20 bits. Second, three cascaded moving-average filters each output the average of the last 64 samples. The data has now been decimated by a factor of 64:1. Third, a half-band FIR filter stage with symmetrical, equal ripple both in the passband and stopband discards half of the output codes to yield output data at the desired 48kHz or 44.1kHz sampling rate at 20 bits of resolution.

Differential Linearity Code Width Histogram
Figure 6



The oversampling architecture used in the **ADC 20048** provides excellent differential linearity performance and eliminates the need for an expensive analog anti-aliasing filter — two major advantages over conventional A/D converters.

Differential Linearity

The differential linearity performance is achieved because, unlike a conventional converter, an output code transition never corresponds to an actual change in analog input voltage. A change in analog input causes the idle pattern at the output of the flash ADC to shift by increasing the frequency of occurrence of one code, while decreasing the frequency of occurrence of another. Since the energy of the idle pattern is somewhat larger than the flash ADC quanitization noise, smooth transitions are guaranteed across the entire analog input range.

Conventional Successive Approximation (SAR) or Multiple-Pass (Subranging) ADC architectures rely on the matching tolerance of resistors or capacitors for their differential linearity performance. The best available 16-bit resolution ADC's that use these technologies achieve approximately ±0.5 LSB typical differential linearity. The **ADC 20048** obtains ±0.2 LSB maximum differential linearity at 20 bits of resolution, which represents a 40:1 improvement.

Both the SAR and subranging ADC's typically have their poorest performance at the bipolar zero-crossing point on their transfer curves due to the tolerance matching of all of the resistors or capacitors used to weight the most significant bits. The **ADC 20048**, again, because no actual code transition corresponds to this zero-crossing point, exhibits superior performance at the zero-crossing point. This preserves the fidelity of low-level signals, critical to audio digitizing.

Differential linearity is measured by recording a histogram representing code density. A histogram of this histogram is calculated, which yields a plot that shows probability of code widths on the vertical scale, and code width on the horizontal scale. *Figure 6* shows a measured example of such a plot.

Anti-Aliasing Filters

With the flash ADC converting at 128 times the actual sampling rate, or approximately 6MHz, no anti-aliasing filter is required. The function of the anti-aliasing filter is provided by the **Decimator**. All frequencies between half and 1.5 times the sampling rate are eliminated by the FIR digital filter stage. The **AFE** low-pass analog filter, plus the cascaded moving average filters eliminate all frequencies above 1.5 times the sampling frequency. Final anti-alias performance is:

F_S=48kHz:
-80dB minimum rejection from 28kHz - 68kHz;
-50dB minimum rejection from 68.1kHz - 1.5MHz

F_S=44.1kHz:
-80dB minimum rejection from 24.1kHz - 64.1kHz;
-50dB minimum rejection from 64.2kHz - 1.5MHz

Integral Linearity

Figure 7a shows the untrimmed integral linearity of a typical **ADC 20048** converter. Worst case untrimmed integral linearity error for this particular converter is ±40 LSB's. An exhaustive, computer-controlled test system is used to trim each **ADC 20048** such that

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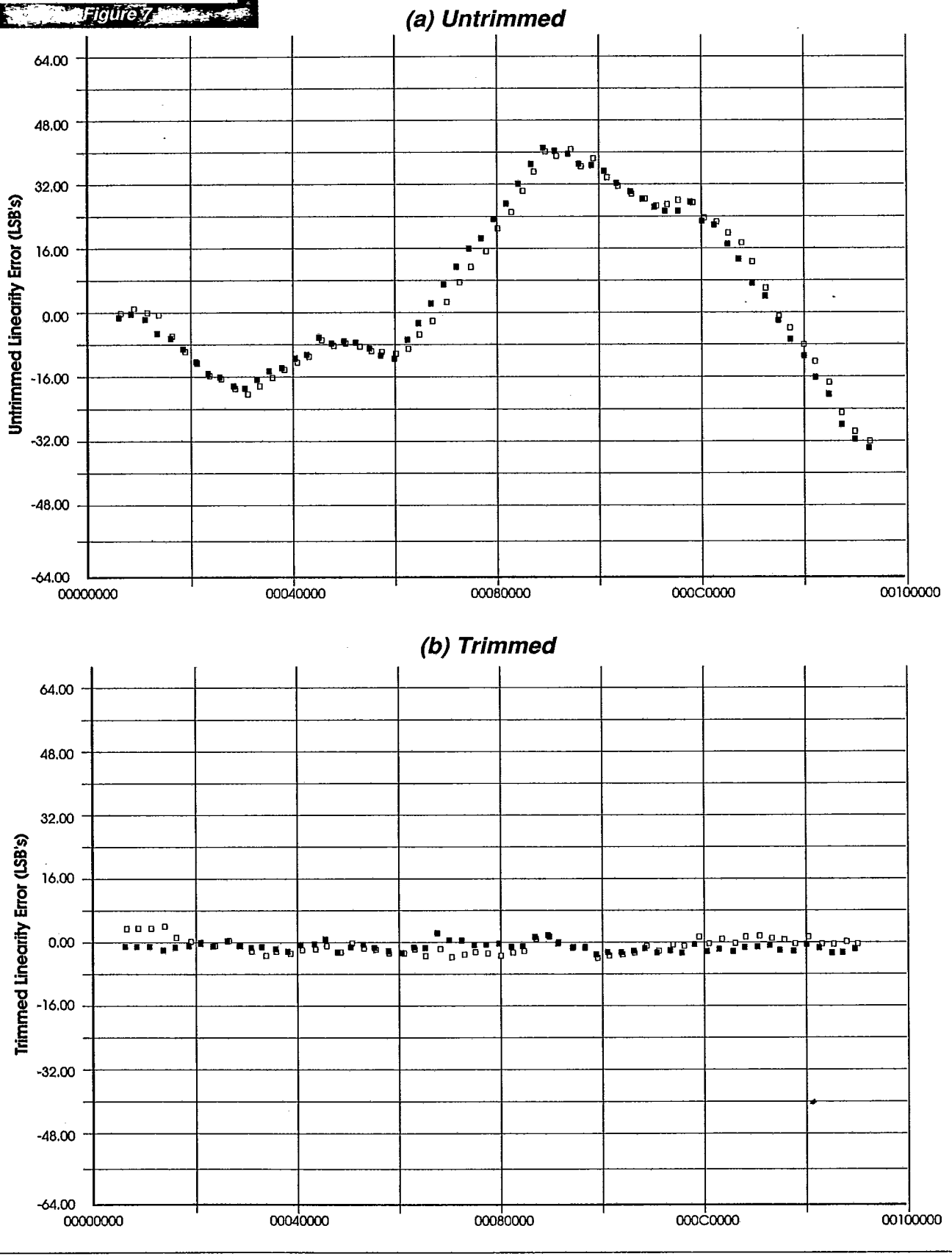
Integral Linearity

Figure 7



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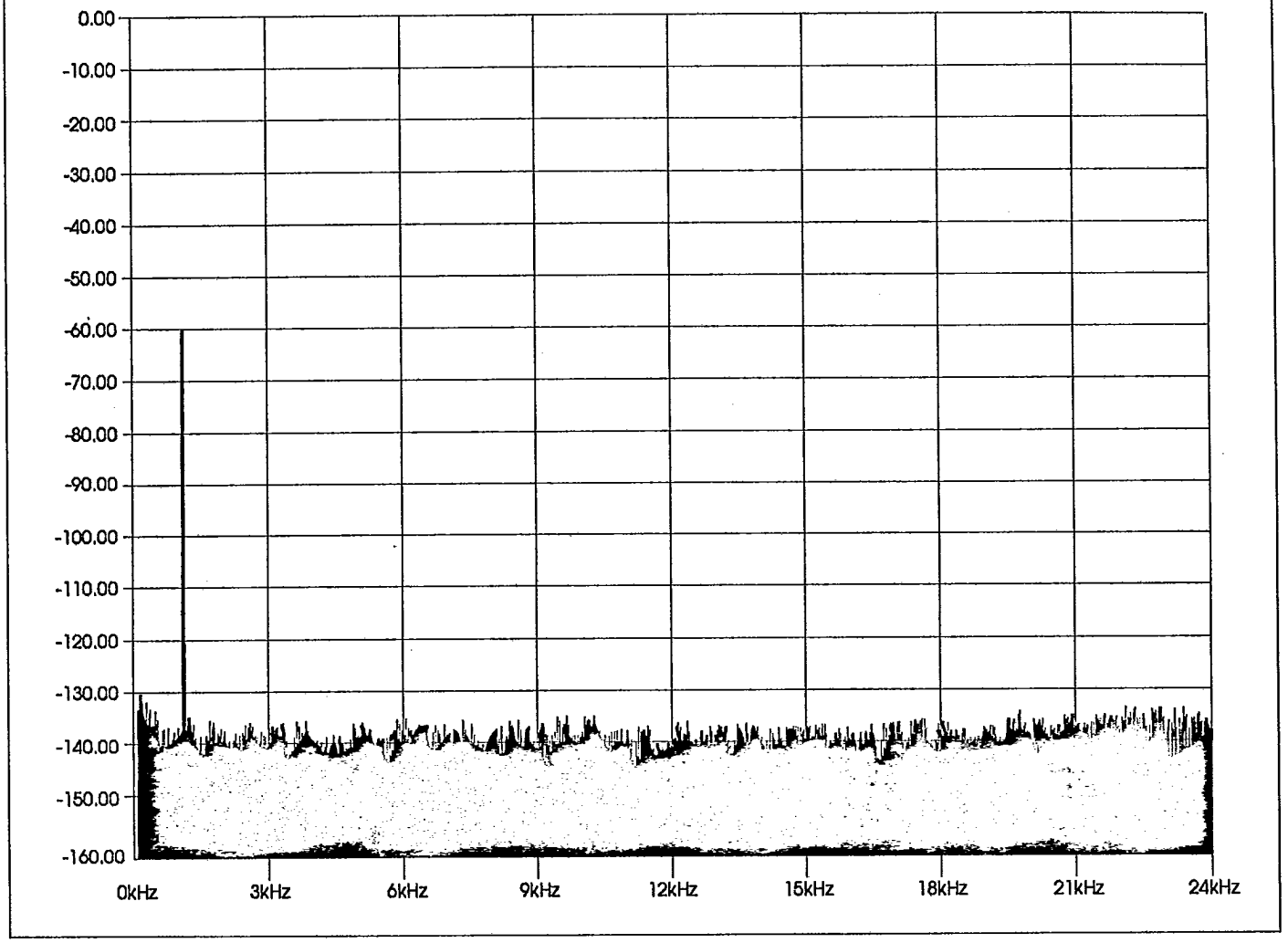
1kHz FFT Plot

Figure 8



the integral linearity is ±4 LSB's at 20-bits resolution. *Figure 7 b* shows the trimmed integral linearity plot for the **ADC 20048**.

Low-level Signal Performance

As previously discussed, the zero-crossing point of the **ADC 20048** doesn't correspond to a major code transition, hence, its performance is significantly better for low-level signals than conventional ADCs. *Figure 8* shows an FFT plot for a 1kHz sinusoidal signal at a -60dB level. Noise and spurious responses are below -130dB. This supports the specified dynamic range with performance that is not achieved by any other converter technology. SAR and subranging ADCs generally exhibit their worst FFT performance with low-level signals.

Hear It For Yourself!!

Eliminating the noise, distortion, phase non-linearity and transient response problems associated with anti-aliasing filters dramatically improves the sound quality of digital recording equipment. **Chesky Records** has recorded numerous Jazz CD's using the 128x oversampling ADC technology, all of which have received uncontested, critical acclaim from numerous reviewers. Among their catalog selections is a sampler Jazz CD that includes digitally recorded comparisons between a 128x oversampling ADC and a conventional ADC used in mastering systems. You are invited to request a copy of the sampler Jazz CD from **UltraAnalog** and hear the difference for yourself.

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Pinout

AFE 20048/D20C10 Pinout

The functions of the various pins of the **AFE 20048 Analog Front -End** and **D20C10 Decimator** are described below. Refer to the mechanical/dimensions drawing on the last page of this data sheet.

AFE 20048 ANALOG FRONT-END

Pins 1, 27, 28, 29, 30, 56, 57, & 58
Not used, make no connection

Pins 2-7 — OUT 0 (LSB) - OUT 5 (MSB)
The parallel output data from the **AFE** at a 6.144MHz data rate.

Pins 8 & 51 — +5V
Power supply voltage input.

Pins 9, 10, 49 & 50 — DGND
Digital Ground.

Pin 11 — $\overline{\text{Power-on-Reset}}$
Signal used by **Decimator** to reset all filters and latches to their power on conditions. Goes low for 1,024 cycles of the MASTER CLOCK INPUT provided 1) the power supplies take less than 50ms to turn on, or 2) the MASTER CLOCK starts 20ms or less after the +15V supply reaches +14.25V. If the user has an existing, on-board master reset, the $\overline{\text{POR}}$ need not be used.

Pins 17/20 — V_{SS} 6M (OUT)/V_{DD} 6M (OUT) —
Power supply outputs required by the 6MHz clock driver outputs in the **Decimator**. These are isolated from the other power supplies to minimize noise due to spike currents from the drivers.

Pin 18 — 6M CLK (IN)
Accepts a 6.144MHz clock signal from the **Decimator**, used for internal conversion timing.

Pin 19 — 6M DLYD (IN)
Accepts a delayed 6.144MHz clock signal from the **Decimator**, used for internal conversion timing.

Pin 21 & 38 — +15V
Analog power supply voltage input.

Pin 22 & 37 — -15V
Analog power supply voltage input.

Pins 23 & 36 — AGND
Analog Ground.

Pin 31 — - INPUT
Inverting (-) analog signal input.

Pin 32 — + INPUT
Non-inverting (+) analog signal input.

Pin 33 — SEL3
Provides optimum filter compensation for flat response with either 48kHz or 44.1kHz data output (sampling) rate. If SEL3 is open, filter response is optimized for 48kHz. If SEL3 is connected to SEL2, filter response is optimized for 44.1kHz.

Pin 34 — SEL2
Used to select both data output (sampling) rate and full scale input range.

Pin 35 — SEL1
Used to select input full scale range; when connected to SEL2, the input full scale range is ±3V; when left open, the input full scale range is ±5V.

D20C10 DECIMATOR FILTER IC

Pin 1 —
Not used. Make no connection.

Pin 2 — WORD CLOCK OUTPUT
This pin supplies a clock at the rate of the MASTER CLOCK ÷ 256. This output clock signal can be tied directly to the **Decimator**'s own SAMPLING RATE CLOCK IN, Pin 3, to supply the required clock input signal.

Pin 3 — SAMPLING RATE CLOCK IN
This input accepts the 48 or 44.1kHz sampling rate clock either 1) derived from and synchronized with the master 12MHz nominal clock, or 2) taken directly from the **Decimator**'s WORD CLOCK OUTPUT, Pin 2.

Pin 4 — $\overline{\text{OE}}$
Enables the **Decimator**'s digital data outputs, OUT0 - OUT19, which are tri-stated; active low, i.e. logic "0" enables outputs.

Pin 5 — FORMAT
Selects output data format; logic "0" selects 2's complement, while logic "1" selects offset binary output data format.

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Pin 6 — $\overline{\text{POR}}$
Active low, must be low for 1,024 MASTER CLOCK cycles. Resets the digital filters and latches to their initial operating state. Can use $\overline{\text{POR}}$ signal generated by **AFE**, or preferably, a system software reset or power monitor output.

Pin 7 — TEST
This pin is used only during factory testing. For proper operation, it should be tied to a logic low ("0"). Do not bring this pin to a logic "1" condition for any reason.

Pins 8/11 — V_{DD} 6M/V_{SS} 6M
Isolated and regulated power developed by the **AFE** is applied to these input pins to power the output buffers that provide the 6M CLOCK and 6M DLYD, 6MHz timing signal outputs of the Decimator.

Pin 9 — 6M DLYD
A 6MHz timing signal output used by the **AFE** for internal timing and synchronization with the **Decimator**. This signal is a delayed version of the 6M CLOCK signal at pin 10.

Pin 10 — 6M CLOCK — A 6MHz timing signal output used by the **AFE** for internal timing and synchronization with the **Decimator**.

Pins 12 & 13/36 & 37 — V_{SS} (CORE)/V_{DD} (CORE)
The power supply inputs for all of the **Decimator** circuitry except the output latches and 6MHz timing signal buffers.

Pin 14 — MODE
Tie to logic high ("1") for proper **Decimator** operation. Used only during factory testing. To avoid permanent damage to the **Decimator**, never allow the logic level on this pin to go low (logic "0").

Pins 15 - 20 — IN5 (MSB) - IN0 (LSB)
Digital inputs to the digital filter chain internal to the **Decimator.**

Pin 21 — MASTER CLOCK IN
Accepts the 12MHz nominal master clock timing reference signal. Pulse width must be controlled as shown in the input timing diagram (*Figure 2*). A single pulse of insufficient width will cause the **Decimator** to enter an illegal state, which will require it to be reset to regain proper operation.

Pin 22 — AUXILLIARY CLOCK OUTPUT
Provides a buffered version of the MASTER CLOCK INPUT signal from pin 21. Not normally used to implement the ADC function.

Pins 23 - 33 — OUT0 (LSB) - OUT10
The lower 11 bits of the parallel 20-bit digital data output word.

Pins 34/35 — V_{SS}/ V_{DD}
The digital ground and +5V power inputs respectively for the output data latches.

Pins 38 - 46 — OUT 11 - OUT 19(MSB)
The most significant nine bits of the parallel 20-bit digital data output word. Pin 46 is OUT 19, which is the MSB.

Pin 47 — SERIAL DATA OUT
This is the 20-bit digital output data in serial form. The data is presented in a 32-bit field with the MSB first. The data is shifted out at the BIT CLOCK rate of 1.536MHz, nominal.

Pin 48 — BIT CLOCK
This clock output is used to synchronize the serial data from the SERIAL DATA OUT, pin 47. The serial data changes state on the high-to-low transition of the BIT CLOCK.

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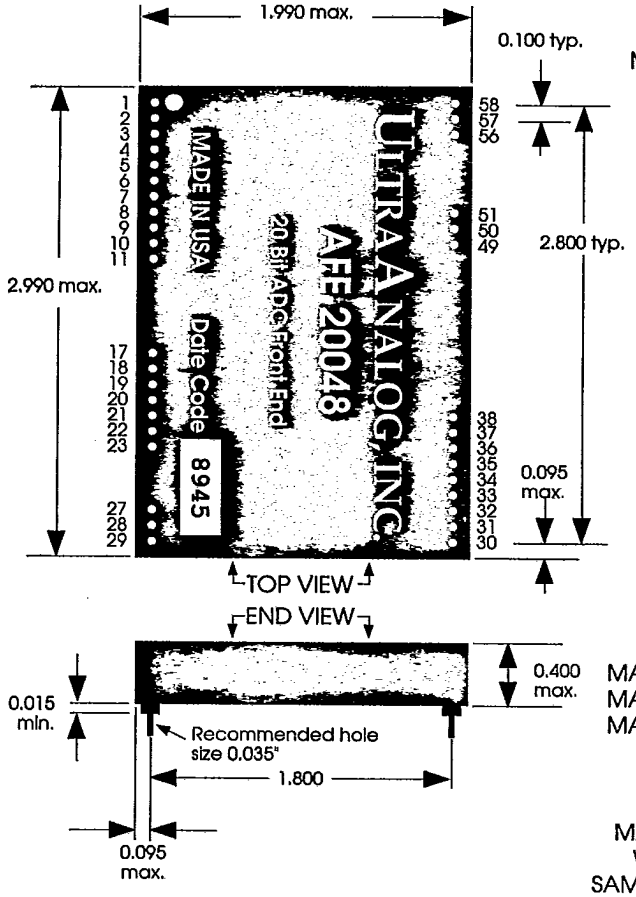
AFE 20048/D20C10 Mechanical

Figure 10



D20C10
TOP VIEW

AFE 20048 Pin Assignments

MAKE NO CONNECTION 1.	58. MAKE NO CONNECTION
OUT 0 (LSB) 2.	57. MAKE NO CONNECTION
OUT 1 3.	56. MAKE NO CONNECTION
OUT 2 4.	
OUT 3 5.	
OUT 4 6.	
OUT 5 (MSB) 7.	
+5V 8.	51. +5V
DGND 9.	50. DGND
DGND 10.	49. DGND
$\overline{\text{POR}}$ 11.	
V_{SS} 6M(OUT) 17.	
6M CLK (IN) 18.	
6M DLYD (IN) 19.	
V_{DD} 6M(OUT) 20.	
+15V 21.	38. +15
-15V 22.	37. -15V
AGND 23.	36. AGND
	35. SEL 1
	34. SEL 2
	33. SEL 3
MAKE NO CONNECTION 27.	32. + INPUT
MAKE NO CONNECTION 28.	31. - INPUT
MAKE NO CONNECTION 29.	30. MAKE NO CONNECTION

D20C10 Pin Assignments

MAKE NO CONNECTION 1.	48. BIT CLOCK
WORD CLOCK OUTPUT 2.	47. SERIAL DATA OUT
SAMPLING RATE CLOCK IN 3.	46. OUT19 (MSB)
OUTPUT ENABLE ($\overline{\text{OE}}$) 4.	45. OUT18
FORMAT 5.	44. OUT17
POR 6.	43. OUT16
TEST 7.	42. OUT15
V_{DD}6M 8.	41. OUT14
6M DLYD 9.	40. OUT13
6M CLOCK 10.	39. OUT12
V_{SS} 6M 11.	38. OUT11
V_{SS} (CORE) 12.	37. V_{DD}(CORE)
V_{SS} (CORE) 13.	36. V_{DD}(CORE)
MODE 14.	35. V_{DD}
IN5 (MSB) 15.	34. V_{SS}
IN4 16.	33. OUT10
IN3 17.	32. OUT9
IN2 18.	31. OUT8
IN1 19.	30. OUT7
IN0 (LSB) 20.	29. OUT6
MASTER CLOCK IN 21.	28. OUT5
AUXILLIARY CLOCK OUTPUT 22.	27. OUT4
OUT0 (LSB) 23.	26. OUT3
OUT1 24.	25. OUT2

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