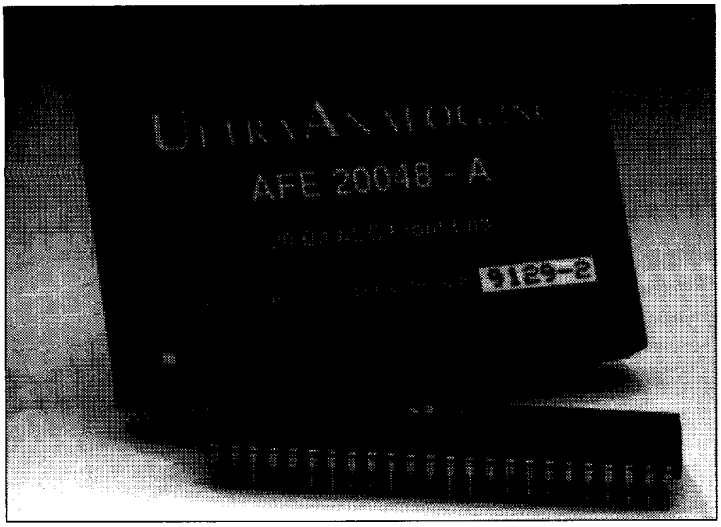


ULTRAANALOG, INC.
Advancing the Analog Art.

T-49-12-09
T-51-10-90

ADC 20048–A

20 Bit Audio ADC
128 x Oversampling

Features

- 20-Bit Resolution
- 108dB Dynamic Range
- 128X Oversampling Rate
- <0.2LSB Diff. Linearity
- Pin-selectable 44.1 or 48kHz Output Data Rates
- Flat Frequency Response to within ±0.05dB
- Pin-selectable ±3V and ±5V Input Ranges

Applications

- Digital Audio Workstations
- Digital Mixing Consoles
- Digital Audio Routing Switchers
- Disk-based Recording
- Microphone Digitizing
- Upgrade 16-Bit Digital Audio Systems
- Sonar
- Analytical Instruments
- MRI Imaging

Description

The **UltraAnalog ADC20048–A** advances the technology in digital audio converters by providing a complete 20-bit Analog-to-Digital Converter in a 2" x 3" shielded module and companion single 48-pin DIP. The **ADC20048–A** architecture features a 128X over–sampling, noise-shaping algorithm that eliminates the need for brick-wall anti-aliasing filters and their associated noise, phase error, distortion and expense. The patented* data conversion algorithm provides **108dB dynamic range**, passband **frequency response** flat to within **±0.05dB**, **-96dB THD and Noise**, and **no differential nonlinearity error** or **harmonic distortion** for low-amplitude signals.

The **ADC20048–A** provides significant improvements in both performance and implementation over the original dbx versions of this ADC architecture. First, the ADC is complete within the **Analog Front-End** (**AFE20048–A**) module and companion (**D20C10**) **Decimator** Filter DIP, requiring only power supply voltages, analog input and master clock signals to operate. All critical analog circuits are packaged within the **AFE** using double-sided, surface-mount technology which provides a highly reliable and economical converter. All of the necessary trimming and alignment, as well as adjustments for offset and distortion null, are done at the factory, using highly advanced, automated testing methods, which correct for all sources of non-linearity error. An internal timing generator provides high immunity to power supply noise which can cause clock jitter. Flat passband frequency response to ±0.05dB is achieved at both 44.1 and 48kHz sampling rates. At sampling rates other than 44.1kHz or 48kHz, the pass–band flatness degrades by ±0.025dB/%. Further, these rates are pin-selectable for ease of system configuration. Finally a differential input with pin-selectable ±3V or ±5V input ranges is provided.

* U.S. patent # 4,588,979

Specifications

ANALOG INPUT

Input Voltage Ranges:	±3V, ±5V
Input Impedance:	Refer to Figure 1
Type:	Refer to Figure 1
CMRR:	60dB min.; dc-20kHz
Offset @ 25°C:	±5mV, max.
Offset Drift:	5 LSBs/°C, typ.; ±5mV max. over full temperature range
Gain Error:	±0.02dB, typ.; ±0.05dB, max.
Gain Drift:	±0.05dB max.over full temperature range

DIGITAL INPUTS

Logic "0":	0V, min.; 1.5V, max.
Logic "1":	3.5V, min.; 5.0V, max.
Input Capacitance:	10pF, max.
Sampling Rate Clock Input:	39.7kHz, min.; 54kHz, max.
Master Clock Input:	256 x sampling rate; 12.288MHz, nominal, for 48kHz data rate; 50±10% duty cycle

DIGITAL OUTPUTS

Logic "0":	0.1V, max.at <1µA; -2.9mA output current
Logic "1":	4.9V, min. at <1µA; +2.9mA output current

DYNAMIC PERFORMANCE

Differential Non-Linearity:	±0.2LSB, typ.
Integral Linearity:	<±0.002% max., 1kHz
THD + Noise:	refer to performance curves
Dynamic Range	-108dB typ.
Frequency Response:	DC-20kHz, ±0.05dB
Passband	
44.1kHz Data Rate:	DC to 21.5kHz (-3dB)
48kHz Data Rate:	DC to 23.5kHz (-3dB)
Stopband	
44.1kHz Data Rate:	24.1kHz to 2.8MHz
48kHz Data Rate:	28kHz to 3.0MHz

POWER REQUIREMENTS [see Note 3]

Power Dissipation:	2.1 watts, typ. with ±15V [see Note 4]
+15.00 ±0.25V:	66mA, typ.
-15.00 ±0.25V:	46mA, typ.
+5.00 ±0.25V:	78mA, typ.

ENVIRONMENTAL

Operating Range:	0°C to +60°C
Storage Range:	-25°C to +85°C
Relative Humidity:	0 to 85%, non-condensing

MECHANICAL

AFE20048–A

Dimensions:	2.05" x 3.05" x 0.46", max.
Material:	High thermal conductivity, black epoxy, polyphenylene sulfide case
Shield:	Critical circuitry internally shielded

D20C10

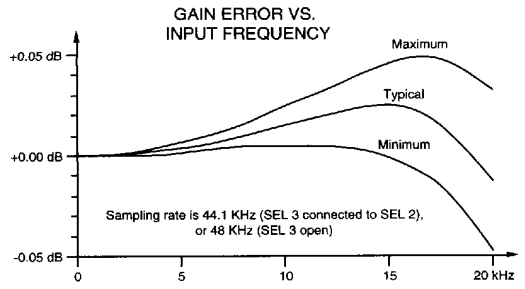
Dimensions:	48-pin plastic DIP
Material:	Epoxy

NOTES

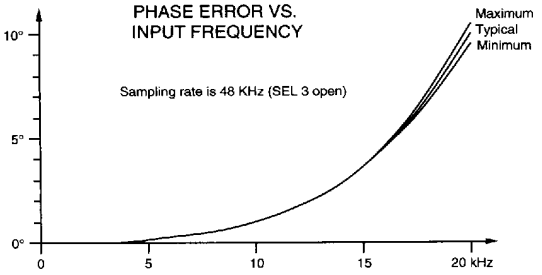
1. All electrical specifications apply to the complete ADC, comprised of the AFE20048–A and D20C10 combination.
2. Dynamic performance characteristics are measured with either sampling frequency of 44.1 or 48kHz.
3. The ±15V power supplies must be linearly regulated. The +5V supply must have less than 20mV$_{p-p}$ switching spikes.
4. A ±12V option dissipates 1.7 watts typical; consult factory.
5. Specifications are subject to change without notice.

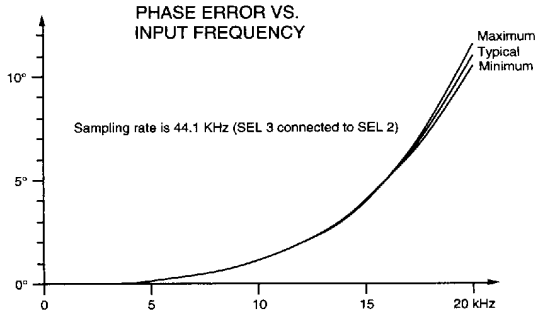
Typical & Maximum Performance Curves

Gain Error vs. Input Frequency

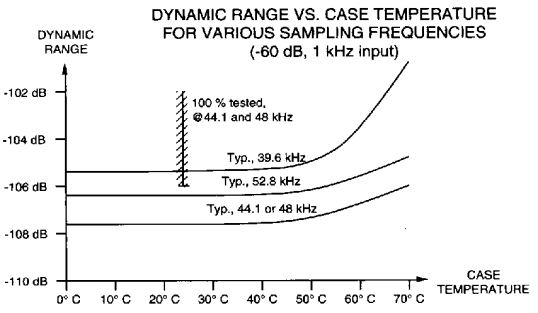


Phase Error vs. Input Frequency

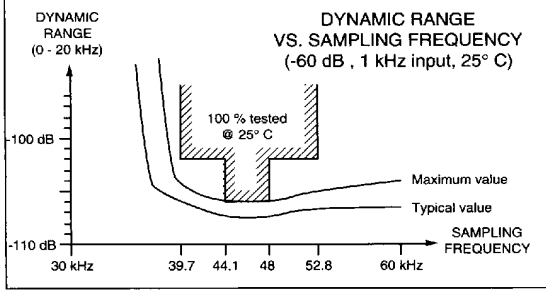




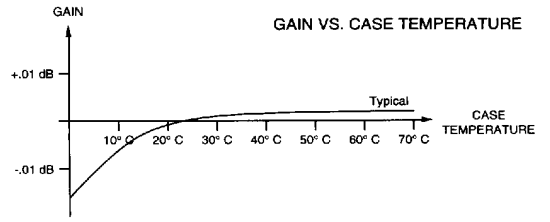
Dynamic Range vs Case Temperature

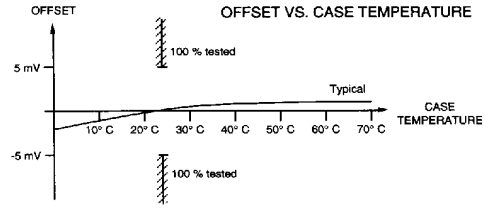


Dynamic Range vs Sampling Frequency

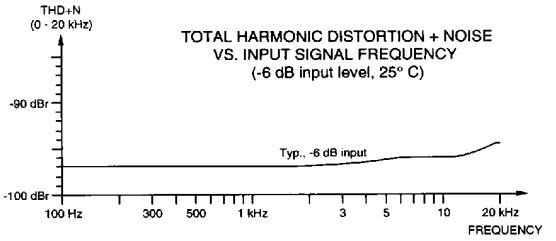


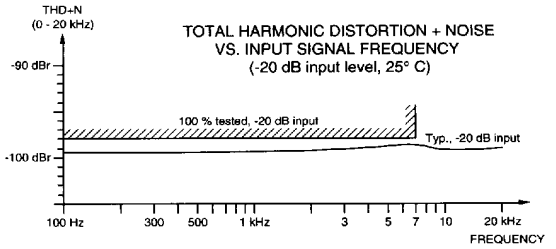
Gain & Offset Error vs.Case Temperature

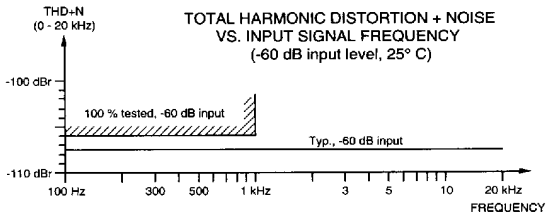




THD + Noise vs. Input Signal Frequency







Principles of Operation

The oversampling architecture used in the **ADC20048–A** provides excellent differential linearity performance and typically eliminates the need for expensive analog anti–aliasing filters — two major advantages over conventional A/D converters.

As shown in *Figure 1*, the **ADC20048–A** consists of the **AFE20048–A** noise–shaping, 128x oversampling ADC and companion **D20C10 Decimator**. The **AFE20048–A** converts the analog signal at 6.144MHz (for 48kHz sample clock) with four (4) bits of resolution. Since the ADC error is noise-shaped, the noise spectrum is very low below 20kHz, and increases significantly with frequency. This 4–bit data is then processed by the decimator in two stages to remove the noise above 20kHz, while decimating down to the sampling rate. The resulting output data has 20 bits of resolution.

AFE20048–A ANALOG FRONT-END

The **AFE20048–A** consists of a differential amplifier, low–pass filter, summing amplifier, noise–shaping filter, 4–bit flash ADC, and 4–bit DAC.

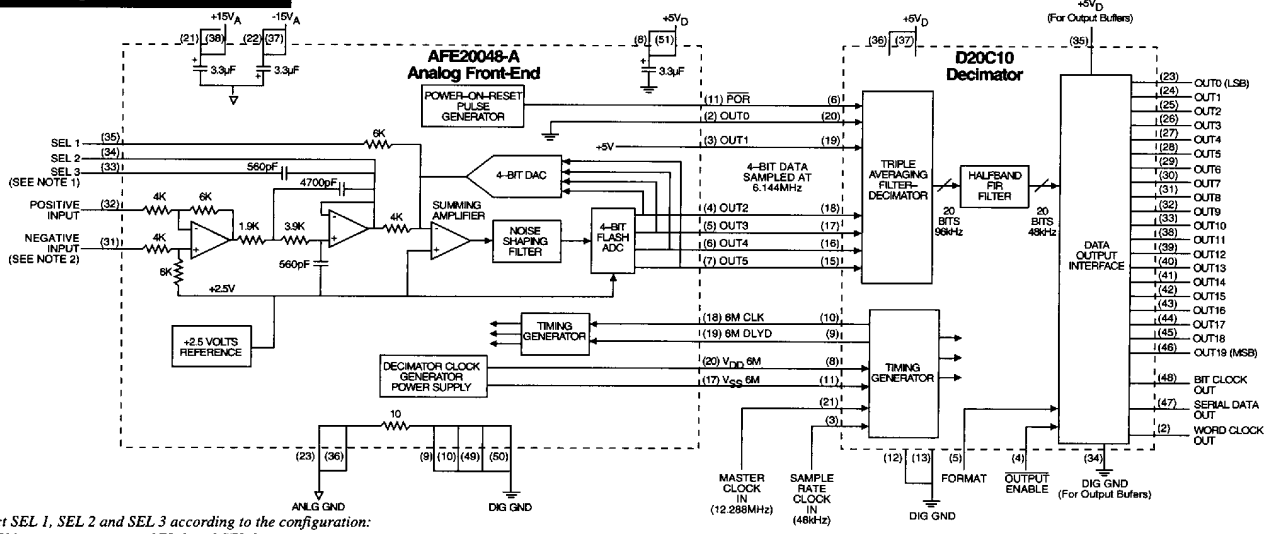
The differential amplifier provides for common–mode noise attenuation. The input may be driven differentially or single–ended without any significant effect on performance of the **ADC20048–A**.

Anti–alias filtering is provided by the 2nd order low–pass filter. The corner frequency is approximately 34kHz, and the response is slightly peaked to compensate for the 1.9dB rolloff at 20kHz by the **D20C10 Decimator**. This compensation results in an overall frequency response that is flat to 20kHz, within ±0.05dB, at either 44.1kHz or 48kHz sample rate.

The output of the low–pass filter is converted by the noise–shaping ADC, which consists of a summing amplifier, noise–shaping filter, 4–bit flash ADC and 4–bit DAC. The analog signal is converted to a 4–bit digital approximation by the flash ADC at a 128x over–sampling rate of 6.144MHz (128 x 48kHz data sampling rate). The output of the flash ADC is applied simultaneously to the **Decimator** and the 4–bit DAC. The DAC output is subtracted from the analog input at the summing amplifier, resulting in an error signal that is integrated by the noise–shaping filter. Since the error signal is integrated, the noise spectrum at the output of the ADC is extremely low in the audio bandwidth, and increases with frequency. The integration of the error signal guarantees that the average digital output of the ADC matches the input signal, within the accuracy of the DAC. With no input signal to the ADC, the output is a random sequence of several contiguous codes, with energy just slightly greater than

ADC20048–A Block Diagram

Figure 1



Notes:

1. *Connect SEL 1, SEL 2 and SEL 3 according to the configuration:*
   For ±3V input range, connect SEL 1 and SEL 2.
   For ±5V input range, do not connect SEL 1 and SEL 2.
   For 44.1kHz operation, connect SEL 2 and SEL 3.
   For 48kHz operation, do not connect SEL 2 and SEL 3.

2. *Both positive and negative inputs have an open voltage of +2.5V. The differential input can be used in a single–ended mode, with either the positive or negative input active, or it can be used in the differential mode. There is no significant performance difference between these modes.*

the ADC quantization noise.

D20C10 DECIMATOR

The **Decimator** accepts the 4–bit data from the **AFE20048–A** and performs two filtering actions. First it removes the out of band noise and increases the resolution to 20 bits, with three cascaded moving-average filters, each outputting the average of the last 64 samples. The data has now been decimated by a factor of 64:1. Second, a half-band FIR filter stage with symmetrical, equal ripple both in the passband and stopband discards half of the output codes to yield output data at the desired 48kHz or 44.1kHz sampling rate at 20 bits of resolution.

The **Decimator** filter characteristics *nearly* approximate an ideal low–pass filter with some rolloff at 20kHz. The analog peaking filter inside the **AFE** is intended to cancel the rolloff at 20kHz in the **D20C10**. With a sample clock operating at 44.1kHz, the peaking of the **AFE** is as follows:

5kHz	+0.14dB
10kHz	+0.55dB
15kHz	+1.25dB
20kHz	+2.24dB

With a sample clock of 48kHz, the peaking at 20kHz is reduced to +1.89dB. With certain "audio test signals", it is possible for a user to unknowingly "clip" the **ADC20048A**. Specifically, if a full–amplitude, 1kHz reference tone is used as a system reference and full–amplitude THD+N tests are performed from DC to 20kHz, the **D20C10** will overload due to the peaking inside the **AFE**. If the test signal amplitude is decreased to less than -2dB (with a 48kHz sampling clock), then the **D20C10** will not clip and high frequency performance measurements can be properly completed. [It should be noted that the large–amplitude THD specifications and internal UltraAnalog production tests are performed with signals below -2dB.]

In most real–life audio applications, a full–amplitude, 1kHz tone may be successfully used as a system reference. Since musical instruments do not generate full amplitude, high frequency signals, only harmonics of lower frequencies would generally be present above approximately 8–10kHz. Since the harmonics have lower amplitude, the **D20C10** will not "clip".

Since the **Decimator** data input accepts six bits, the two LSB's of the six bits sent to the **Decimator** are hard–wired inside the **AFE** as a 1–0 combination. Given the 2's complement format of the input word to the **Decimator**, this has the following desired effect — with 0Volts input, which corresponds to mid–scale, the 4–bit output pattern of the ADC itself would produce equal probability of "7" or "8" codes, with a few "6's" and "9's" mised in. With the fifth and sixth bits added in at 1–0, respectively, the 2's complement words have an average value of zero, which produces zero, or half–scale in a binary mode. This is the desired output for a 0Volt input.

Differential Linearity

The differential linearity performance is achieved because, unlike a conventional converter, an output code transition never corresponds to an actual change in analog input voltage. A change in analog input causes the idle pattern at the output of the flash ADC to shift by increasing the frequency of occurrence of one code, while decreasing the frequency of occurrence of another. Since the energy of the idle pattern is somewhat larger than the flash ADC quantization noise, smooth transitions are guaranteed across the entire analog input range.

Conventional Successive Approximation (SAR) or Multiple-Pass (Subranging) ADC architectures rely on the matching tolerance of resistors or capacitors for their differential linearity performance. The best available 16-bit resolution ADC's that use these technologies achieve approximately ±0.5 LSB *typical* differential linearity. The **ADC20048–A** obtains ±0.2 LSB differential linearity *at 20 bits of resolution*, which represents a 40:1 improvement.

Both the SAR and subranging ADC's typically have their poorest performance at the bipolar zero-crossing point on their transfer curves due to the tolerance matching of the resistors or capacitors used to weight the most significant bits. The **ADC20048–A**, again, because no actual code transition corresponds to this zero-crossing point, exhibits superior performance at the zero-crossing point. This preserves the fidelity of low-level signals, critical to audio digitizing.

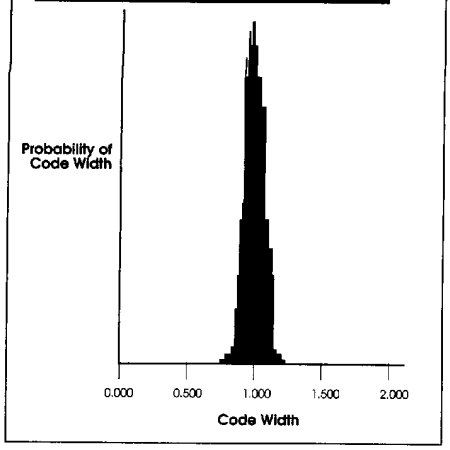
Differential linearity is measured by recording a histogram representing code density. A histogram of this histogram is calculated, which yields a plot that shows probability of code widths on the vertical scale, and code width on the horizontal scale. *Figure 2* shows a measured example of such a plot.

Anti-Aliasing Filters

With the flash ADC converting at 128 times the actual sampling rate, or approximately 6MHz, an external anti–aliasing filter is usually not required. Alias filtering is provided by the analog low–pass filter in the **AFE20048–A** and by the **Decimator**. All frequencies between half and 1.5 times the sampling rate are eliminated by the FIR digital filter stage. The **AFE** low-pass analog filter, plus the cascaded moving average filters eliminate all frequencies above 1.5 times the sampling frequency. Final anti-

Differential Linearity Code Width Histogram

Figure 2



alias performance is:

F_S=48kHz:
-80dB minimum rejection from 28kHz - 68kHz;
-50dB minimum rejection from 68.1kHz - 1.5MHz

F_S=44.1kHz:
-80dB minimum rejection from 24.1kHz - 64.1kHz;
-50dB minimum rejection from 64.2kHz - 1.5MHz

Integral Linearity

Figure 3a shows the untrimmed integral linearity of a typical **ADC20048–A** converter. Worst case untrimmed integral linearity error for this particular converter is ±40 LSB's. An exhaustive, computer-controlled test system is used to trim each **ADC20048–A** such that the integral linearity is ±8 LSB's typical at 20-bits resolution. *Figure 3b* shows the trimmed integral linearity plot for the **ADC20048–A**.

Low-level Signal Performance

As previously discussed, the zero-crossing point of the **ADC20048–A** doesn't correspond to a major code transition, hence, its performance is significantly better for low-level signals than conventional ADCs. The figures on *Page 3* provide THD+Noise plots at various input signal levels.

Hear It For Yourself!!

Eliminating the noise, distortion, phase non-linearity and transient response problems associated with anti-aliasing filters dramatically improves the sound quality of digital recording equipment. Numerous record companies now record with UltraAnalog ADCs, including **Chesky**, **Sony Classical**, **Telarc**, **Capitol**, **Elektra**, **MCA**, **RCA**, and **Warner Brothers**. We invite you to hear the difference for yourself.

Interconnections

Figure 4, "AFE20048–A/Decimator D20C10 Interconnection" shows the complete interconnection scheme to implement a stereo 20-bit ADC converter using two each of the **AFE20048–A Analog Front-End (AFE)** and **D20C10 Decimator** Filter IC.

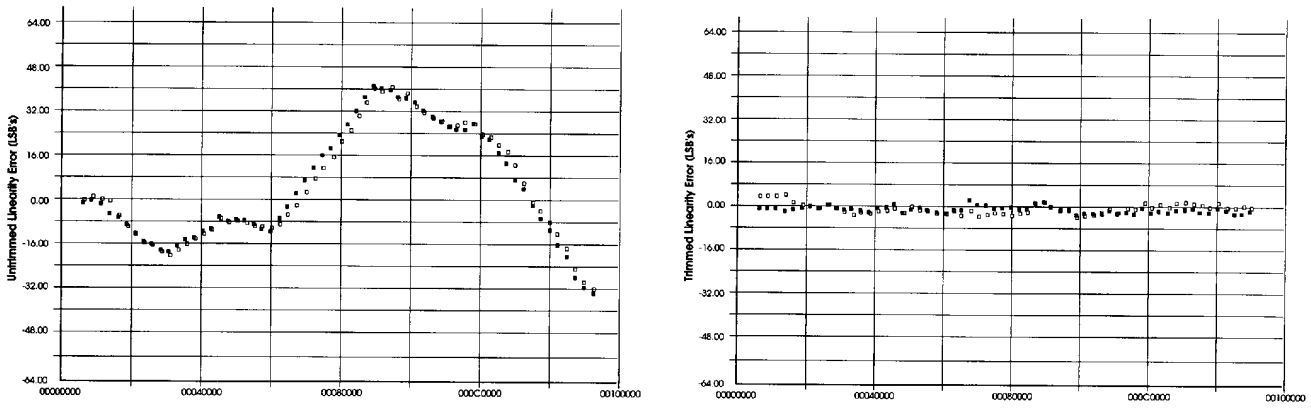
Power Supplies

The **AFE** requires three operating supply voltages, +15V ±0.25V, -15V ± 0.25V and +5V ±0.25V. The ±15V sources must be linearly regulated. Bypass capacitors are not required on the power supply lines, since they are included inside the **AFE**.

The **Decimator** provides separate power and ground pins for the parallel data output buffer. The +5V and ground connected to pins 36, 37,12, and 13 should be the same +5V and ground that is used to power the **AFE20048–A**. If the parallel data output is used, the +5V and ground connected to pins 34 and 35 should be a separate supply, such as the supply used for the digital support circuitry. If the parallel data output is not used, it is not critical which

Integral Linearity

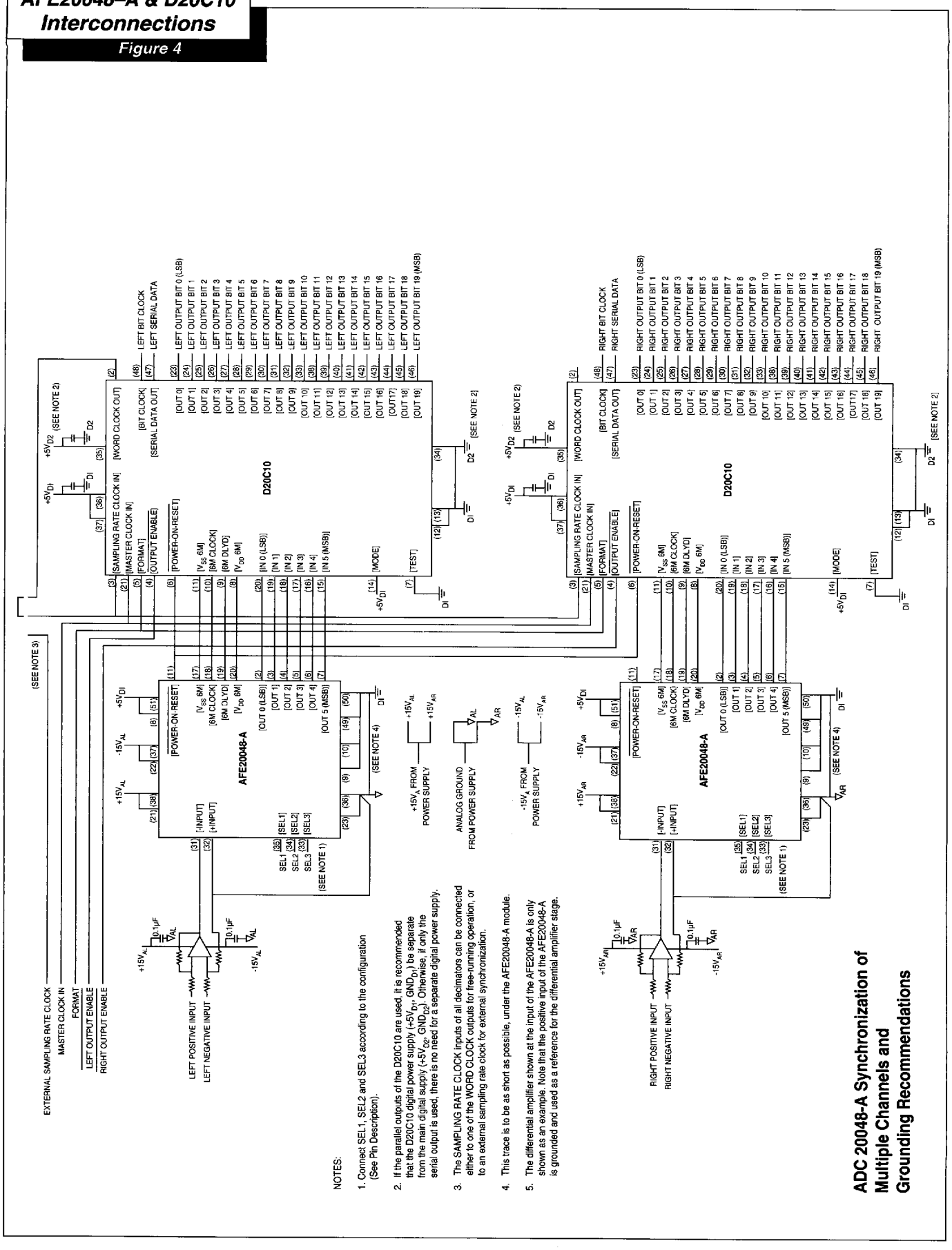
Figure 3



(a) Untrimmed ***(b) Trimmed***

AFE20048–A & D20C10 Interconnections

Figure 4



+5V and ground is connected to pins 34 and 35.

Digital I/O

The digital I/O of the **AFE** and **Decimator** are connected as shown in *Figure 4.* Lead lengths should be as short as possible, with extensive use of ground plane under both the **AFE** and the **Decimator**. Analog and digital grounds are internally tied together in the **AFE**. If desired, the WORD CLOCK OUT (pin 2) from the **Decimator** may be used to drive the SAMPLING RATE CLOCK INPUT (pin 3) of the **Decimator** directly; otherwise, a clock equal to the sampling rate, synchronized to the MASTER CLOCK INPUT per the timing diagrams in *Figure 5, "ADC20048–A Input Timing"* must be provided.

I/O Format Options

Several pin-selectable options are provided relative to analog input full scale range, digital output data sampling rate and format. The input full scale range is normally ±5V. A ±3V input full scale range is selected by an external jumper between **AFE** pin 35, SEL 1 and pin 34, SEL 2. Digital output data sampling rate is normally 48kHz. It can be set to 44.1kHz by a jumper between **AFE** pin 34, SEL 2 and pin 33, SEL 3. The digital output data format is set by logic level on the **Decimator** FORMAT pin (5). A logic low ("0") sets the output data to a 2's complement format, while a logic high ("1") sets the output data to offset binary.

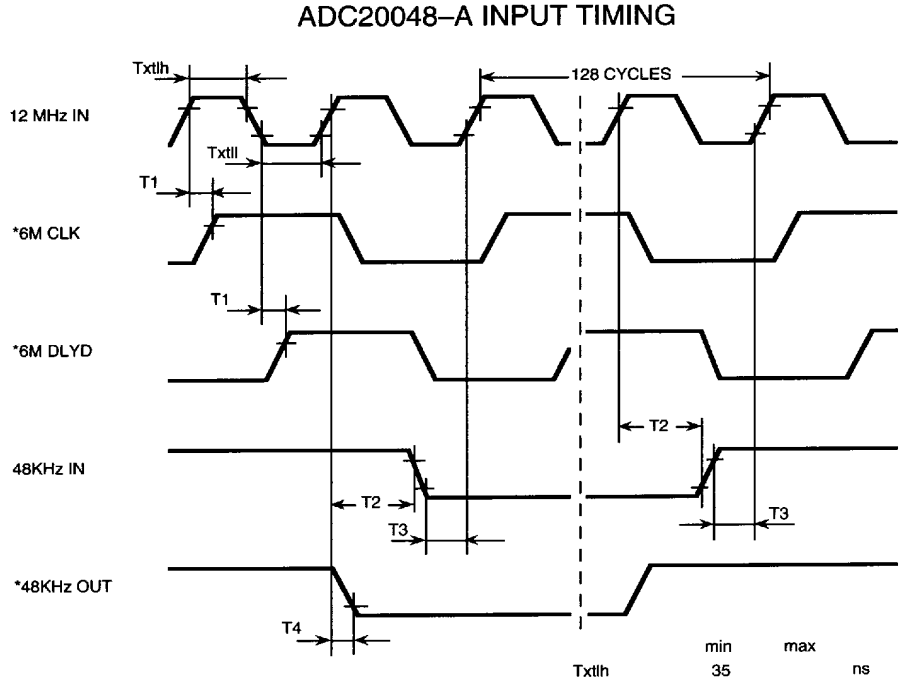
Sampling Rates and Required Clock Signals

Sampling rates other than 48kHz or 44.1kHz can be used, provided they are within the range of 39.7–54kHz. To use a sampling rate other than the two jumper–selectable rates, simply adjust the frequency of the master clock to be 256 x the desired sampling rate (e.g. for a 50.0kHz sampling rate, the master clock frequency would be 50.0kHz x 256 = 12.8MHz). For sampling rates from 40-46kHz, jumper between pin 34, SEL 2 and pin 33, SEL 3 on the **AFE**. For sampling rates from 46-54kHz, do not install any selection jumper. This optimizes the roll-off characteristics of the ADC20048–A to be as close to ideal as possible, although at sampling rates other than 44.1 or 48kHz, a small amount of roll-off or peaking at 20kHz will occur.

Options are also available relative to providing the sampling rate clock signals required by the **Decimator**, and for synchronizing multiple **ADC20048–A** subsystems in multi-channel applications. The **Decimator** requires a precise sampling rate clock input, synchronized to the master 12MHz nominal clock. This sampling rate clock, which is equal to the desired output data rate, must be applied to pin 3,

ADC20048–A Input Timing

Figure 5

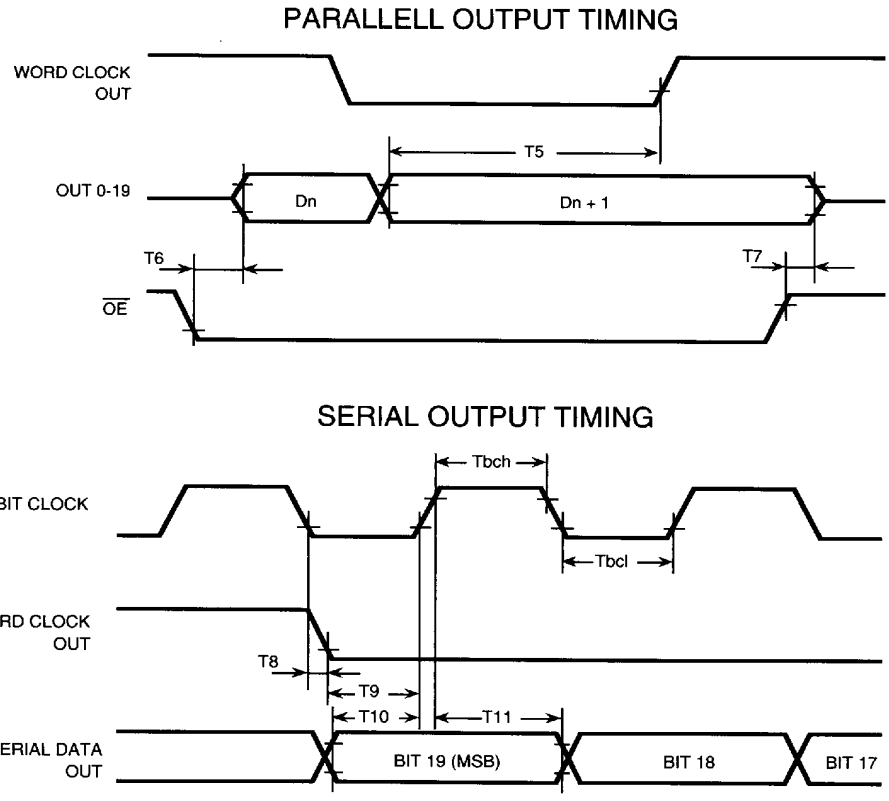


	min	max	
Txtlh	35		ns
Txtll	35		ns
T1		40	ns
T2	0		ns
T3	10		ns
T4	0	40	ns

* Shown for reference only.

Output Data Timing

Figure 6



	min	max	
T5	9000		ns
T6		45	ns
T7		65	ns
Tbch	280		ns
Tbcl	280		ns
T8	0	40	ns
T9	240		ns
T10	225		ns
T11	225		ns

SAMPLING RATE CLOCK IN. Its frequency is MASTER CLOCK ÷256. The **Decimator** itself produces this signal at its WORD CLOCK OUT, pin 2. Unless there is a system-level reason to generate the sampling rate clock signal from the master 12MHz clock signal elsewhere in the system, simply tying the WORD CLOCK OUT and SAMPLING RATE CLOCK IN pins together satisfies this signal requirement.

Serial Data Output

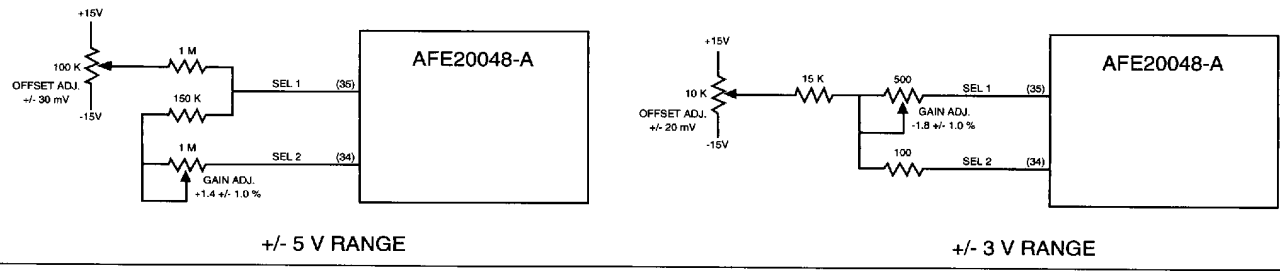
Serial output data is presented on the SERIAL DATA OUT pin (47), synchronized with the BIT CLOCK output on pin 48. The data is output as a 32-bit field, MSB first, with the last 12 bits set to zero. The data changes state on the high-to-low transition of the BIT CLOCK signal. The bit clock frequency is 32 times the sampling rate clock. Thus, for a 48kHz data sampling rate, the bit clock is 32x48kHz, or 1.536MHz. *Figure 6, "Serial Output Timing"* shows the timing relationship for serial data output from the **ADC20048–A**.

Parallel Data Output

A logic low ("0") on pin 4, the OE (OUTPUT ENABLE) enables the tri-state output latches and presents the data on the output pins. The 20-bit parallel data outputs, pins 23 (LSB) to 33 and 38 to 46 (MSB), are

AFE20048–A Offset/Gain Adjust

Figure 7



Pinout

disabled by a logic high ("1"). The timing relationships for parallel data output are shown in *Figure 6, "Parallel Output Timing".*

Synchronizing Multiple ADC20048–A's

Multiple **AFE20048–A** and **D20C10** subsystems in a multi-channel system can be synchronized by connecting the master 12MHz clock signal to pin 21, MASTER CLOCK INPUT of each **Decimator**. If necessary, several non-inverting buffers in parallel can be used to increase the drive capability of the master clock signal for connecting to large numbers of **ADC 20048–A** without loading down the master clock source. The WORD CLOCK OUT from one of the **Decimators** may be connected to the SAMPLING RATE CLOCK IN on each of the **Decimators**.

Pinout

The functions of the various pins of the **AFE20048–A Analog Front–End** and **D20C10 Decimator** are described below. Refer to the mechanical/dimensions drawing on *Page 12* of this data sheet.

AFE 20048 ANALOG FRONT-END

Pins 1, 27, 28, 29, 30, 56, 57, & 58
Not used, make no connection

Pins 2-7 — OUT 0 (LSB) – OUT 5 (MSB)
The parallel output data from the **AFE** at a 6.144MHz data rate.

Pins 8 & 51 — +5V
Power supply voltage input.

Pins 9, 10, 49 & 50 — DGND
Digital Ground.

Pin 11 — $\overline{\text{Power-on-Reset}}$ (Out)
Signal used by **Decimator** to reset all filters and latches to their power on conditions. Goes low for 1,024 cycles of the MASTER CLOCK INPUT provided 1) the power supplies take less than 50ms to turn on, or 2) the MASTER CLOCK starts 20ms or less after the +15V supply reaches +14.25V. If the user has an existing, on-board master reset, the $\overline{\text{POR}}$ need not be used.

Pins 17/20 — V_{SS} 6M (OUT)/V_{DD} 6M (OUT) —
Power supply outputs required by the 6MHz clock driver outputs in the **Decimator**. These are isolated from the other power supplies to minimize noise due to spike currents from the drivers.

Pin 18 — 6M CLK (IN)
Accepts a 6.144MHz clock signal from the **Decimator**, used for internal conversion timing.

Pin 19 — 6M DLYD (IN)
Accepts a delayed 6.144MHz clock signal from the **Decimator**, used for internal conversion timing.

Pin 21 & 38 — +15V
Analog power supply voltage input.

Pin 22 & 37 — -15V
Analog power supply voltage input.

Pins 23 & 36 — AGND
Analog Ground.

Pin 31 — - INPUT
Inverting (-) analog signal input.

Pin 32 — + INPUT
Non-inverting (+) analog signal input.

Pin 33 — SEL3
Provides optimum filter compensation for flat response with either 48kHz or 44.1kHz data output (sampling) rate. If SEL3 is open, filter response is optimized for 48kHz. If SEL3 is connected to SEL2, filter response is optimized for 44.1kHz.

Pin 34 — SEL2
Used to select both data output (sampling) rate and full scale input range.

Pin 35 — SEL1
Used to select input full scale range; when connected to SEL2, the input full scale range is ±3V; when left open, the input full scale range is ±5V.

D20C10 DECIMATOR FILTER IC

Pin 1 — No connection
Not used. Make no connection.

Pin 2 — WORD CLOCK OUTPUT
This pin supplies a clock at the rate of the MASTER CLOCK ÷ 256. This output clock signal can be tied directly to the **Decimator**'s own SAMPLING RATE CLOCK IN, Pin 3, to supply the required clock input signal. The clock on this pin is valid regardless of the status of the $\overline{\text{POR}}$ (power–on–reset) pin (6).

Pin 3 — SAMPLING RATE CLOCK IN
This input accepts the 48 or 44.1kHz sampling rate clock either 1) derived from and synchronized with the master 12MHz nominal clock, or 2) taken directly from the **Decimator**'s WORD CLOCK OUTPUT, Pin 2. A valid sampling rate clock must be presented on this input for at least one sampling cycle before the $\overline{\text{POR}}$ (power–on–reset) pin goes high.

Pin 4 — $\overline{\text{OE}}$(OUTPUT ENABLE)
Enables the **Decimator**'s digital data outputs, OUT0 to OUT19, which are tri-stated; active low, i.e. logic "0" enables outputs.

Pin 5 — FORMAT
Selects output data format; logic "0" selects 2's complement, while logic "1" selects offset binary output data format.

Pin 6 — $\overline{\text{RESET}}$
Active low, must be low for 1,024 MASTER CLOCK cycles. Resets the digital filters and latches to their initial operating state. After each interruption to the master clock, such as may occur during a frequency switch, the power–on–reset must be reasserted (low) for at least 1024 cycles of the master clock. See *Figure 8* for the timing requirements and recom-

mended implementation. In some applications, the master clock is never interrupted once power is turned on; in these cases, the **AFE20048–A** pin 11 (power–on–reset) may be connected to pin 6 of the **Deceimator**.

Pin 7 — TEST
This pin is used only during factory testing. For proper operation, it should be tied to a logic low ("0"). Do not bring this pin to a logic "1" condition for any reason.

Pins 8/11 — V_{DD} 6M/V_{SS} 6M
Isolated and regulated power developed by the **AFE** is applied to these input pins to power the output buffers that provide the 6M CLOCK and 6M DLYD, 6MHz timing signal outputs of the Decimator.

Pin 9 — 6M DLYD
A 6MHz timing signal output used by the **AFE** for internal timing and synchronization with the **Decimator**. This signal is a delayed version of the 6M CLOCK signal at pin 10. This signal is synchronized with the sampling rate clock in (pin 3).

Pin 10 — 6M CLOCK — A 6MHz timing signal output used by the **AFE** for internal timing and synchronization with the **Decimator**.This signal is synchronized with the sampling rate clock in (pin 3).

Pins 12 & 13/36 & 37 — V_{SS} (CORE)/V_{DD} (CORE)
The power supply inputs for all of the **Decimator** circuitry except the output latches and 6MHz timing signal buffers.

Pin 14 — MODE
Tie to logic high ("1") for proper **Decimator** operation. Used only during factory testing. To avoid permanent damage to the **Decimator**, never allow the logic level on this pin to go low (logic "0").

Pins 15 - 20 — IN5 (MSB) - IN0 (LSB)
Digital inputs to the digital filter chain internal to the **Decimator**.

Pin 21 — MASTER CLOCK IN
Accepts the 12MHz nominal master clock timing reference signal. Pulse width must be controlled as shown in the input timing diagram (*Figure 5*). A single pulse of insufficient width will cause the **Decimator** to enter an illegal state, which will require it to be reset to regain proper operation.

Pin 22 — AUXILIARY CLOCK OUTPUT
Provides a buffered version of the MASTER CLOCK INPUT signal from pin 21. Not normally used to implement the ADC function.

Pins 23 - 33 — OUT0 (LSB) - OUT10
The lower 11 bits of the parallel 20-bit digital data output word.

Pins 34/35 — V_{SS}/ V_{DD}
The digital ground and +5V power inputs respectively for the output data latches. Must be powered regardless of whether or not the output latches are used.

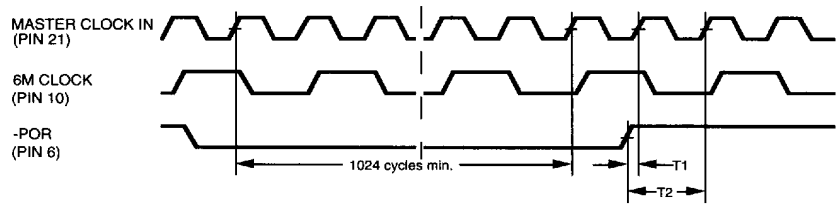
Pins 38 - 46 — OUT 11 - OUT 19(MSB)
The most significant nine bits of the parallel 20-bit digital data output word. Pin 46 is OUT 19, which is the MSB.

Pin 47 — SERIAL DATA OUT
This is the 20-bit digital output data in serial form. The data is presented in a 32-bit field with the MSB first. The data is shifted out at the BIT CLOCK rate of 1.536MHz, nominal.

Pin 48 — BIT CLOCK
This clock output is used to synchronize the serial data from the SERIAL DATA OUT, pin 47. The serial data changes state on the high-to-low transition of the BIT CLOCK.

Decimator Reset Timing

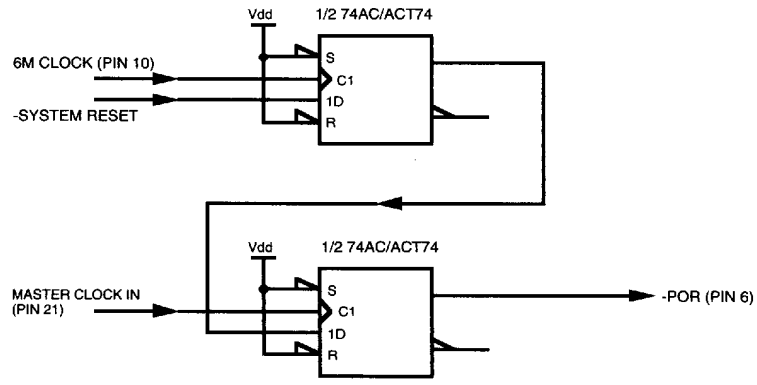
Figure 8



T1 = 20ns max.

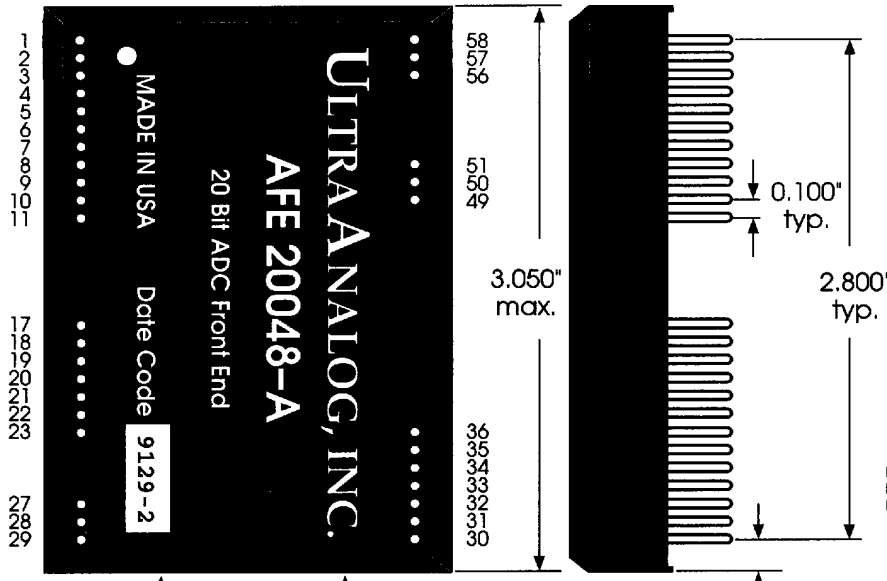
T2 = 60ns min.

SUGGESTED EXTERNAL -POR CIRCUIT



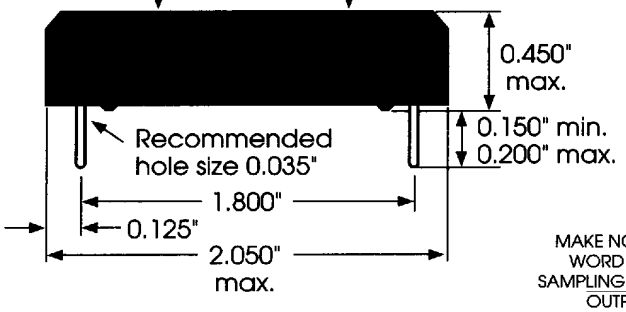
AFE 20048–A & D20C10 Mechanical

Figure 9



AFE 20048–A Pin Assignments

MAKE NO CONNECTION 1.	58. MAKE NO CONNECTION
OUT 0 (LSB) 2.	57. MAKE NO CONNECTION
OUT 1 3.	56. MAKE NO CONNECTION
OUT 2 4.	
OUT 3 5.	
OUT 4 6.	
OUT 5 (MSB) 7.	
+5V 8.	51. +5V
DGND 9.	50. DGND
DGND 10.	49. DGND
POR 11.	
V_{SS} 6M(OUT) 17.	
6M CLK (IN) 18.	
6M DLYD (IN) 19.	
V_{DD} 6M(OUT) 20.	
+15V 21.	38. +15
-15V 22.	37. -15V
AGND 23.	36. AGND
	35. SEL 1
	34. SEL 2
	33. SEL 3
MAKE NO CONNECTION 27.	32. + INPUT
MAKE NO CONNECTION 28.	31. - INPUT
MAKE NO CONNECTION 29.	30. MAKE NO CONNECTION



D20C10 Pin Assignments

MAKE NO CONNECTION 1.	48. BIT CLOCK
WORD CLOCK OUTPUT 2.	47. SERIAL DATA OUT
SAMPLING RATE CLOCK IN 3.	46. OUT19 (MSB)
OUTPUT ENABLE (OE) 4.	45. OUT18
FORMAT 5.	44. OUT17
RESET 6.	43. OUT16
TEST 7.	42. OUT15
V_{DD}6M 8.	41. OUT14
6M DLYD 9.	40. OUT13
6M CLOCK 10.	39. OUT12
V_{SS} 6M 11.	38. OUT11
V_{SS} (CORE) 12.	37. V_{DD}(CORE)
V_{SS} (CORE) 13.	36. V_{DD}(CORE)
MODE 14.	35. V_{DD}
IN5 (MSB) 15.	34. V_{SS}
IN4 16.	33. OUT10
IN3 17.	32. OUT9
IN2 18.	31. OUT8
IN1 19.	30. OUT7
IN0 (LSB) 20.	29. OUT6
MASTER CLOCK IN 21.	28. OUT5
AUXILLIARY CLOCK OUTPUT 22.	27. OUT4
OUT0 (LSB) 23.	26. OUT3
OUT1 24.	25. OUT2

D20C10
TOP
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