ULTRA ANALOG, INC.
Advancing the Analog Art.

Rev. 1

T-49-12-90

AES20

Ultra-Low Jitter AES/EBU Receiver

FEATURES

- 40 ps intrinsic jitter
- 1 kHz jitter attenuation corner frequency
- AES/EBU and SPDIF formats
- Internal low-jitter D flip-flop
- Transformer isolated
- 16, 18, 20 and 24 bits data output formats
- 28 to 55 kHz sampling rates

DESCRIPTION

The UltraAnalog AES20 is a complete AES/EBU and SPDIF receiver. It is designed to provide the jitter performance required by today's high-resolution digital-to-analog and analog-to-digital converters, performance not yet possible in monolithic circuits. In a 1.65 x 2.05" (41 x 52 mm) shielded module, the AES20 provides the following functions:

- data extraction,
- control and user bits extraction,
- actual incoming frequency measurement,
- error detection and reporting,
- low jitter clock generation and regeneration.

In addition, the AES20 has impedance matched, transformer isolated inputs for both AES and SPDIF signals, therefore reducing the number of required external components.

SPECIFICATIONS

AES INPUT (refer to Fig. 2)

Input voltage range	+/- 3 V to +/- 10 V
Differential impedance	110 Ohm (refer to Fig. 3)
Common mode impedance	equivalent to 4 pF max.
Isolation	200 VAC min.

SPDIF INPUT	
Input voltage range	+/- .2 V to +/- 2 V
Differential impedance	75 Ohm (refer to Fig. 4)
Common mode impedance	equivalent to 4 pF max.
Isolation	200 VAC min.
DIGITAL INPUTS	
Low input voltage	.8 V max.
High input voltage	2 V min.
Input current	+/- 10 uA max.
Input capacitance	15 pF max.
DIGITAL OUTPUTS	
Low output voltage	40 V max. @ 3.2 mA
High output voltage	3.75 V min. @ -200 uA
AKIN INPUT	
Low input voltage	1.5 V max.
High input voltage	3.5 V min.
Input current	+/- 10 uA max.
Input capacitance	10 pF max.
AKOUT OUTPUT	
Low output voltage	.10 V max. @ 3.2 mA
High output voltage	4.65 V min. @ -3.2 mA
JITTER PERFORMANCE	
Intrinsic jitter	40 ps typ. for Fs = 44.1 or 48 kHz
(20-40,000 Hz)	(refer to Fig. 5)
Jitter attenuation cut-off frequency	1 kHz max. (refer to Fig. 6)
POWER REQUIREMENTS	
+15.00 +/- .25 V analog	75 mA typ.
-15.00 +/- .25 V analog	4 mA typ.
+5.00 +/- .25 V digital	80 mA typ.
Power dissipation	1.585 W typ.
ENVIRONMENTAL	
Operating range	0 to 60 degrees C
Storage range	-25 to 85 degrees C
MECHANICAL	
Dimensions	1.65 x 2.05 x .046" max. 41.01 x 52.07 x 11.69 mm max.
Material	High thermal conductivity epoxy in polyphenylene sulfide case
Shielding	Low jitter circuitry completely shielded in solid brass

PRINCIPLES OF OPERATION

As shown on Fig. 1, the AES20 consists of an isolation input stage, a fast phase-lock-loop (PLL), a decoding circuitry, a frequency measurement circuit, a low-jitter PLL and a D-type flip-flop.

The isolation input stage is best described by Fig. 2. The AES input is transformer isolated, with a 110 Ohm differential impedance practically independent of frequency (refer to Fig. 3). The SPDIF input is also transformer isolated, with a 75 ohm differential impedance almost independent of frequency (refer to Fig. 4). The transformer capacitance (primary to secondary) is specified to be less than 4 pF.

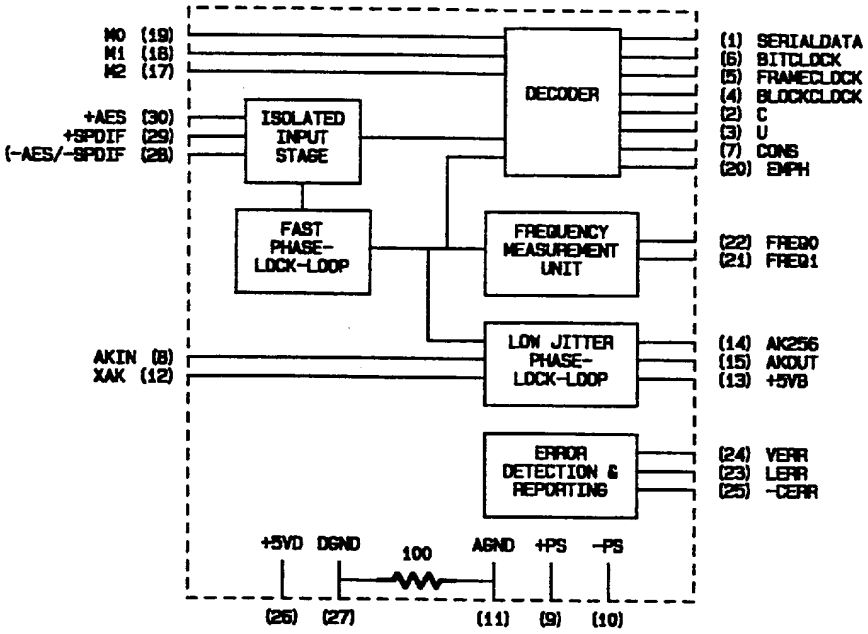

Fig. 1 AES20 BLOCK DIAGRAM

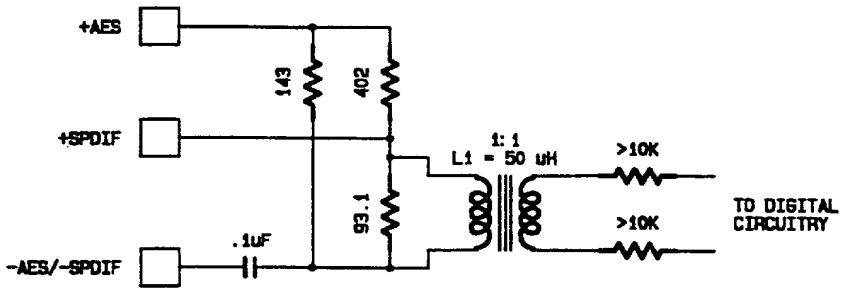

Fig. 2 INPUT STAGE SCHEMATIC

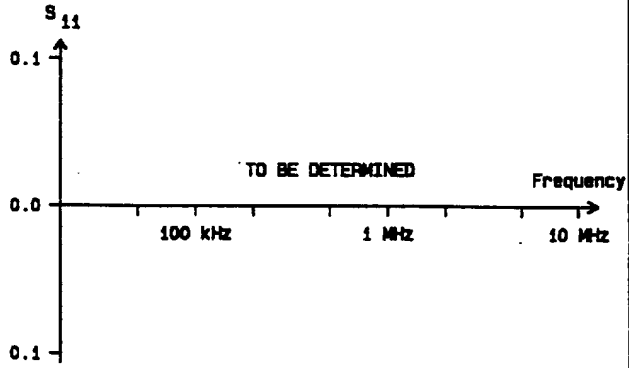

Fig. 3 AES INPUT REFLECTION COEFFICIENT IN A 110 OHM TRANSMISSION LINE

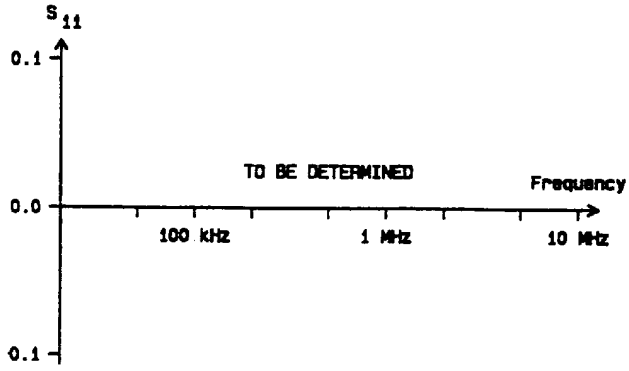

Fig. 4 SPDIF INPUT REFLECTION COEFFICIENT IN A 75 OHM TRANSMISSION LINE

The fast phase-lock-loop recovers from the input stream a clock whit a frequency equal to 256 times the sampling frequency (256 Fs). This clock is powered by the digital supply, and is used by the decoder.

The decoder extracts data from the input stream. It also extracts the user and control bits. Biphase compliance and parity flags are verified, and for professional applications, the CRC is checked. Data is output in one of five different formats, depending on the setting of the three mode inputs M2, M1 and M0. Please refer to Fig. 7 and 8 for timing diagrams. In addition, two control bits are decoded on output pins:

- CONS is high for consumer mode, low for professional mode,
- EMPH is high in the following cases:
  - in professional mode, 50/15 us or CCITT J17 emphasis is encoded in the input,
  - in consumer mode, emphasis is encoded in the input.

  EMPH is low in the other cases:
  - in professional mode, no emphasis is encoded or emphasis is not specified in the input,
  - in consumer mode, no emphasis is encoded in the input.

The frequency measurement circuit compares the clock provided by the fast PLL to an internal crystal oscillator. To reduce jitter, the crystal oscillator is turned off after the measurement is made. The frequency is measured at power-up, after each sudden frequency change, after each biphase coding error and after each parity error. Measuring the input signal frequency with a crystal yields a much more reliable information than decoding control bits 6 and 7. The frequency is presented on pins FREQ1 and FREQ0 in a format compatible with most popular digital oversampling filters:

	FREQ1	FREQ0
32 kHz +/- 4 %	1	1
44.1 kHz +/- 4 %	0	0
48 kHz +/- 4 %	1	0
Out of these ranges	1	0

The low-jitter phase-lock-loop is an independent circuit powered by the analog supply. It locks on the output of the fast PLL, and its long time constant (160 us min.) filters out incoming jitter frequencies above 1 kHz (refer to Fig. 6). The voltage-controlled-oscillator, which is the most sensitive part of the module, is entirely enclosed in a solid brass shield. Its output, AK256, has a frequency equal to 256 times the sampling frequency (256 Fs), and is referenced to the analog ground.

Most users use an oversampling digital filter to improve the DAC performance. They are then confronted with the problem of generating a jitter free oversampling clock. The filter generates an oversampling clock, but it is contaminated with jitter due to the noise present inside the digital circuitry. Using a D-type flip-flop to synchronize this oversampling clock, its jitter can be made as low as that of the 256 Fs clock recovered by the AES20. Such a D-type flip-flop is included in the AES20, both for ease of application and to guarantee jitter integrity. Typically, the "Deglitch" output of the digital filter is connected to the flip-flop input AKIN and the output AKOUT is used as the DAC deglitching clock. AKOUT is referenced to the analog ground.

Some DACs do not have a deglitching circuit, and rely on good internal transition characteristics. Such a DAC needs a jitter-free signal on its "Load" input, i.e. the input that internally transfers parallel data from the shift register to the DAC portion of the integrated circuit. The AKOUT pin will typically be used to drive this "Load" input.

Three error flags are presented by the AES20:

- VERR goes high when one of the following four conditions is met:
  - the fast PLL is out of lock,
  - a biphase violation occurred,
  - a parity error occurred,
  - the current sample is marked invalid (validity flag = 1).

  This bit is updated twice per sample.

- LERR goes high when one of the following four conditions is met:
  - the low-jitter PLL is out of lock,
  - the fast PLL is out of lock,
  - a biphase violation occurred,
  - a parity error occurred.

  When activated, this bit is guaranteed to stay high for at least two blocks (8 ms @ Fs = 48 kHz).

- -CERR goes low in the professional mode when a CRC error occurred. -CERR is defined only when LERR is low. When LERR is low, this bit is updated every block (250 times per second @ Fs = 48 kHz)

JITTER

For each transition of a physical signal, there is a difference between the actual transition time and its expected (ideal) time. The sequence of these differences is called jitter. Like any time sequence, jitter has a frequency spectrum. It can be shown that jitter frequencies above 40 kHz, when interfering with audio signals below 20 kHz inside a DAC (see note 1), produce error signals outside the 0-20 kHz audio band. Therefore, the designer needs to be concerned only with jitter frequencies below 40 kHz.

Like in any AES receiver, there are two main sources of jitter in the AES20. The first one is the intrinsic jitter of the receiver, i.e. the output jitter using a jitter-free input, and the second one is the transmitted jitter, i.e. the portion of the input jitter not attenuated by the receiver.

The AES20, by providing a clock with an typical intrinsic jitter of 40 ps, far exceeds the performance of current monolithic circuits. More importantly, perhaps, it attenuates incoming jitter at frequencies above 1 kHz, making the design much less sensitive to externally supplied signal sources than it would be with current monolithic circuits. Please refer to Fig. 5 and 6 for more detail.

The application note AP-03 goes into more detail about this topic.

Note 1: This applies only to DACs and oversampling filters in which the oversampling quantization noise is of the same order of magnitude as the input signal resolution. It does not apply to 1 bit DACs, for instance.

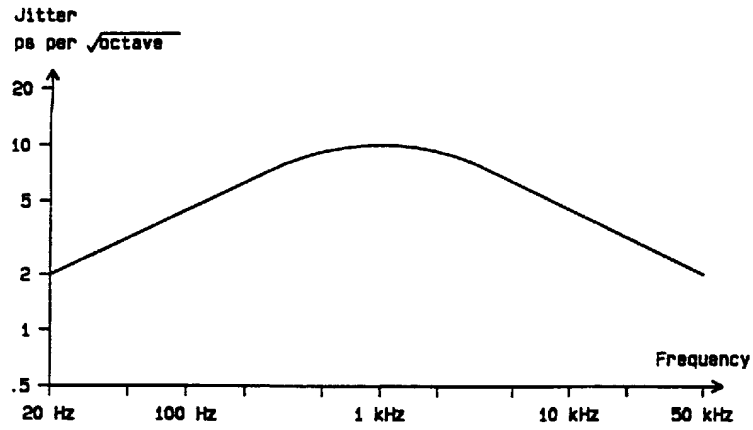

Fig. 5 INTRINSIC JITTER SPECTRUM

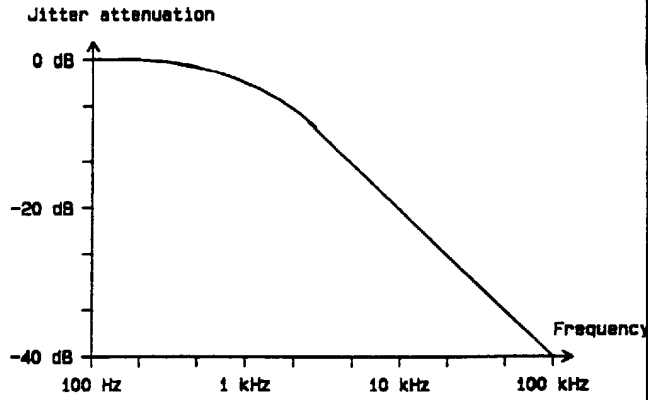

Fig. 6 JITTER ATTENUATION VS FREQUENCY

PIN DESCRIPTION

+5VD, DGND (Pins 26 and 27):
Digital power supply, +5 V and ground.

+PS, -PS, AGND (Pins 9, 10 and 11):
Analog power supply, +15 V, -15 V and ground. The analog and the digital ground are isolated by a 100 ohm resistor.

+AES, -AES/-SPDIF (Pins 30 and 28):
Isolated AES inputs.

+SPDIF (Pin 29):
This input is used in lieu of +AES for SPDIF signals.

M0, M1, M2 (Pins 19, 18 and 17):
These inputs select the serial output mode.

FRAMECLOCK (Pin 5):
This output is the sampling clock.

BITCLOCK (Pin 6):
This output marks the data bit transitions.

SERIALDATA (Pin 1):
This output contains the audio data.

BLOCKCLOCK (Pin 4):
This output is high for the first four frames of each AES block and low for the other 20 frames.

AK256 (Pin 14):
The 256 Fs low-jitter output.

+5VB (Pin 13):
This output is a logical high level to be used with XAK only.

XAK (Pin 12):
This input, when brought to a high level, causes the AK256 clock to be internally inverted. It only affects the timing of the AK256 and AKOUT signals. All other digital outputs remain unchanged. This pin is used to better control the synchronization between a digital processor/filter and a sample and hold. This input must be connected either to AGND or to +5VB.

AKIN, AKOUT (Pins 8 and 15):
The input AKIN is internally reclocked by the AES20 at a 256 Fs rate and output on the AKOUT pin. This reclocking greatly reduces any jitter present on the AKIN line.

LERR, VERR, -CERR (Pins 23, 24 and 25):
These error indicator outputs are described in section 1.4.

FREQ0, FREQ1 (Pins 22 and 21):
These frequency indicator outputs are described in section 1.3.

C, U (Pins 2 and 3):
These serial outputs carry the control and user bits as defined in the AES specifications.

CONS (Pin 7)
This output is high when the incoming signal reflects a consumer interface.

EMPH (Pin 20)
This output is high when the incoming signal reflects that emphasis has been added.

Pin assignment diagram:

Pin 1 SERIALDATA	Pin 30 +AES
Pin 2 C	Pin 29 +SPDIF
Pin 3 U	Pin 28 -AES/-SPDIF
Pin 4 BLOCKCLOCK	Pin 27 DGND
Pin 5 FRAMECLOCK	Pin 26 +5VD
Pin 6 BITCLOCK	Pin 25 -CERR
Pin 7 CONS	Pin 24 VERR
Pin 8 AKIN	Pin 23 LERR
Pin 9 +PS	Pin 22 FREQ0
Pin 10 -PS	Pin 21 FREQ1
Pin 11 AGND	Pin 20 EMPH
Pin 12 XAK	Pin 19 M0
Pin 13 +5VB	Pin 18 M1
Pin 14 AK256	Pin 17 M2
Pin 15 AKOUT	No pin 16

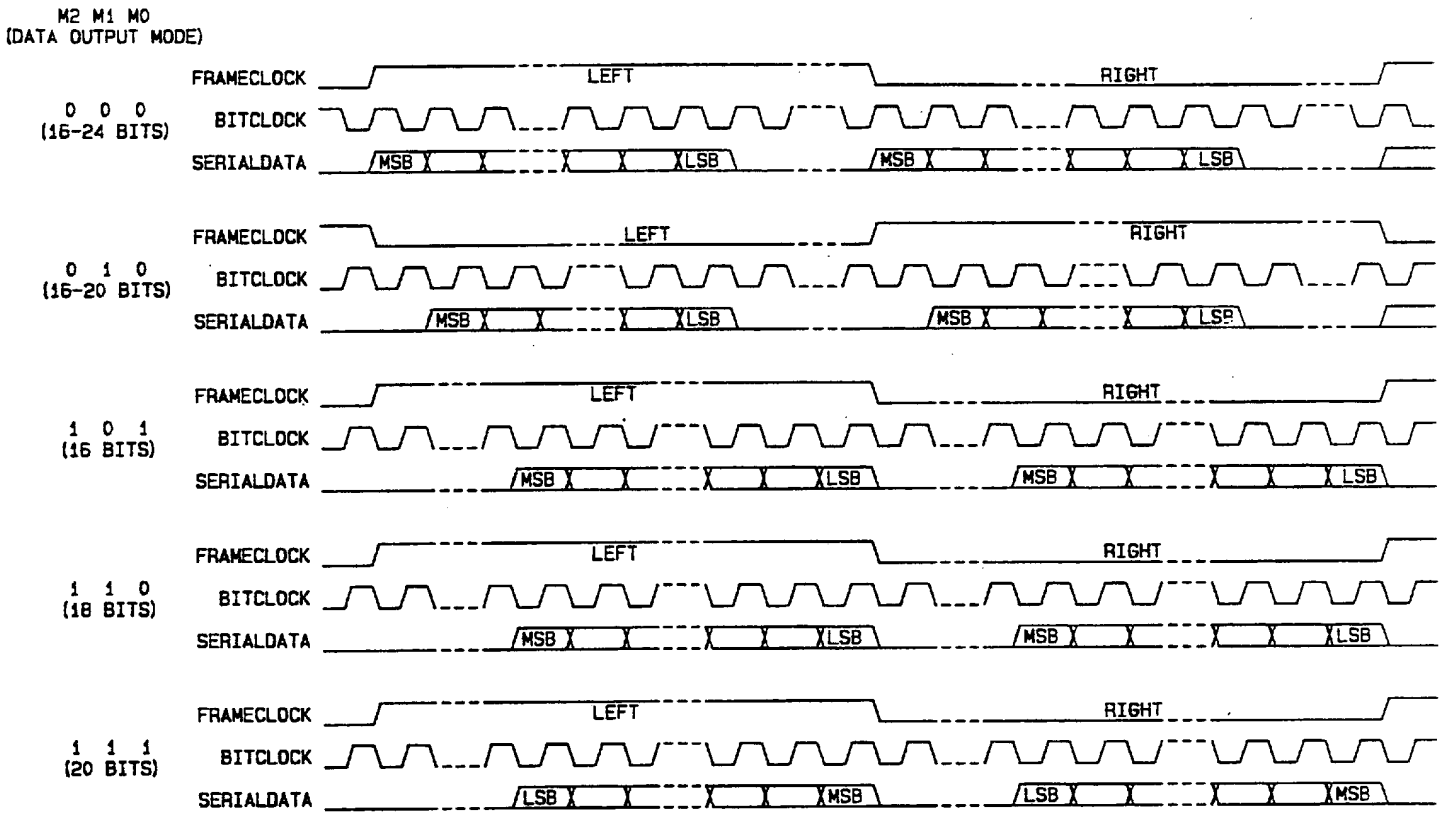

Fig. 7 DATA OUTPUT FORMATS

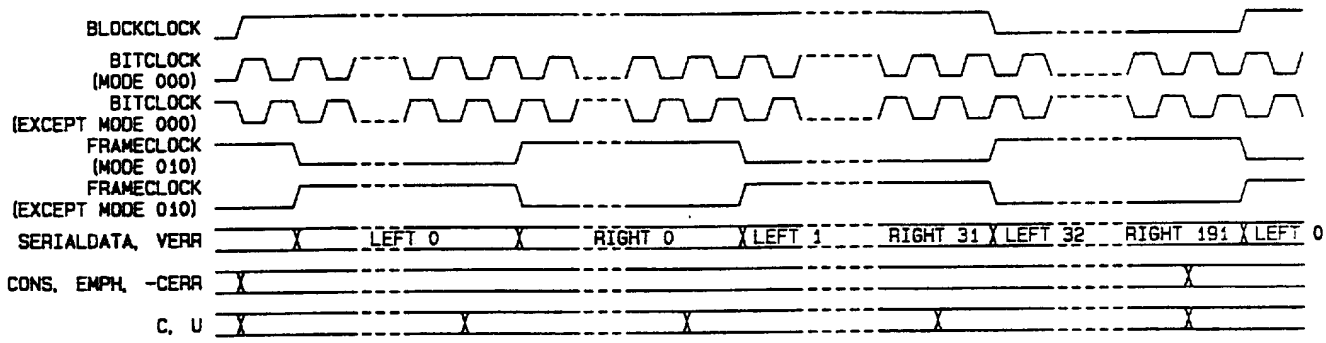

Fig. 8 CLOCKS AND DATA TIMING

APPLICATION HINTS

Proper grounding is vital to all analog designs. While it is not possible to establish grounding rules valid for all possible applications of the AES20, the following information may prove useful.

The "Hold" signal, for DAC which have a track-and-hold, or the "Load" signal, for DAC which do not, must be kept jitter-free. This is why the AKOUT output of the AES20 is referenced to the analog ground, and this is also why the HOLD input of the UltraAnalog DACD20400, DACD20400-A or DAC20 is referenced to the analog ground. Unfortunately, the "Load" input of most monolithic converters is not.

One simple way to avoid jitter contamination in both cases is to connect the analog power supplies and ground of the AES20 directly to the analog power supplies and ground of the DAC(s). The analog and digital grounds of the AES20 are isolated from each other by a 100 Ohm resistor, and so no ground loop is created. The AES20 analog power and ground pins supply only the low-jitter section of the module, i.e. the circuitry generating AK256 and AKOUT and therefore do not get contaminated by any digital signal, or by the jitter on the incoming signal. It is safe to power them together with other analog circuits such as DACs and amplifiers.

Fig. 11 through 14 show typical application schematics for the AES20.

TO BE DETERMINED

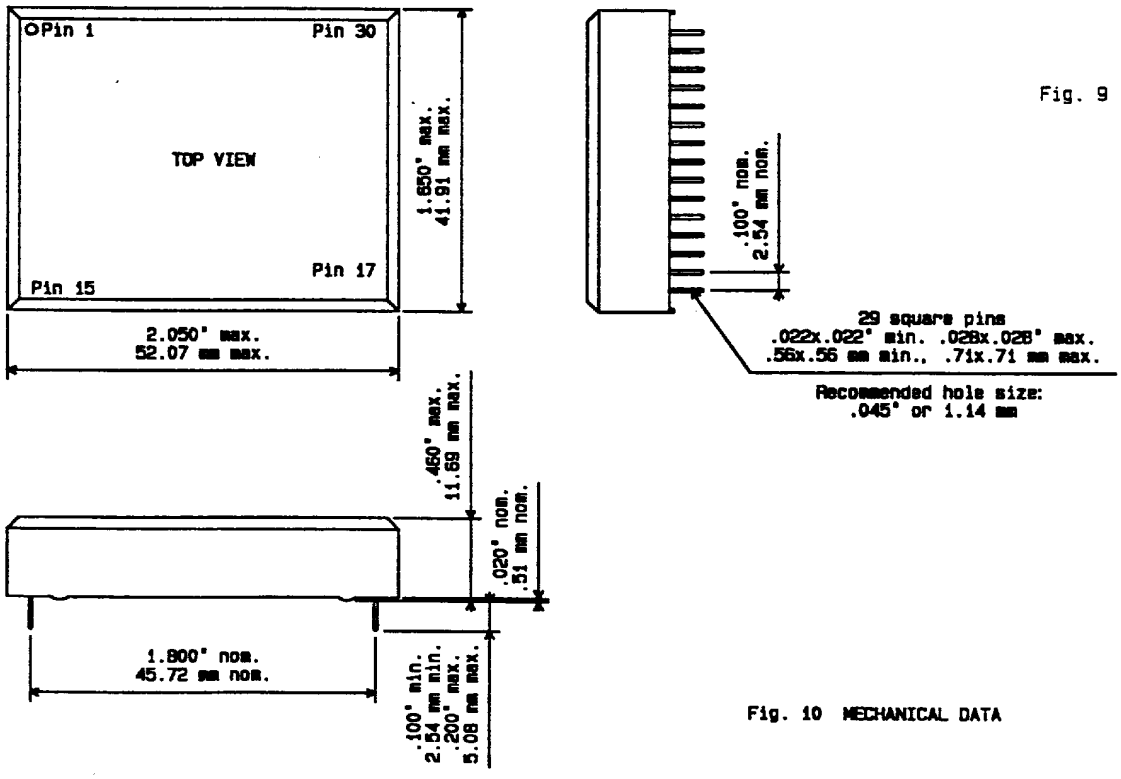

Fig. 9 CLOCK TIMING

Fig. 10 MECHANICAL DATA

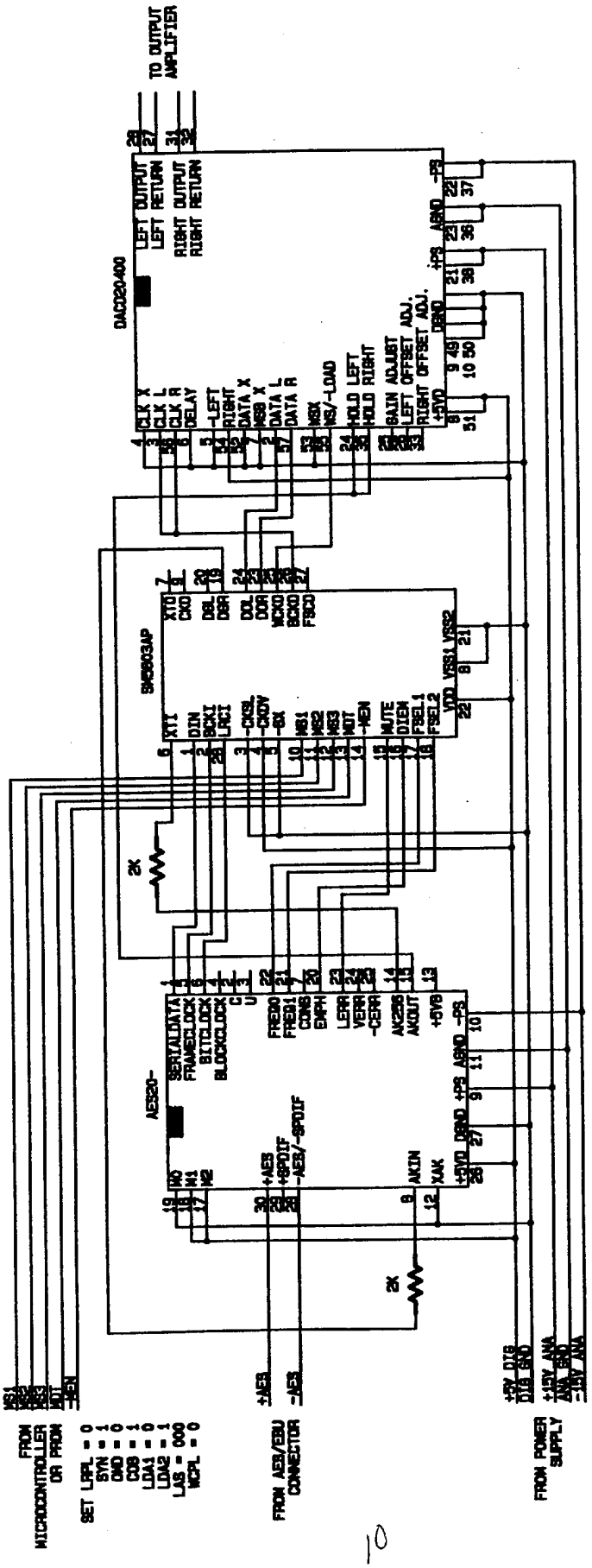

Fig. 11 AES20 USED WITH SM5803 AND DAC020400

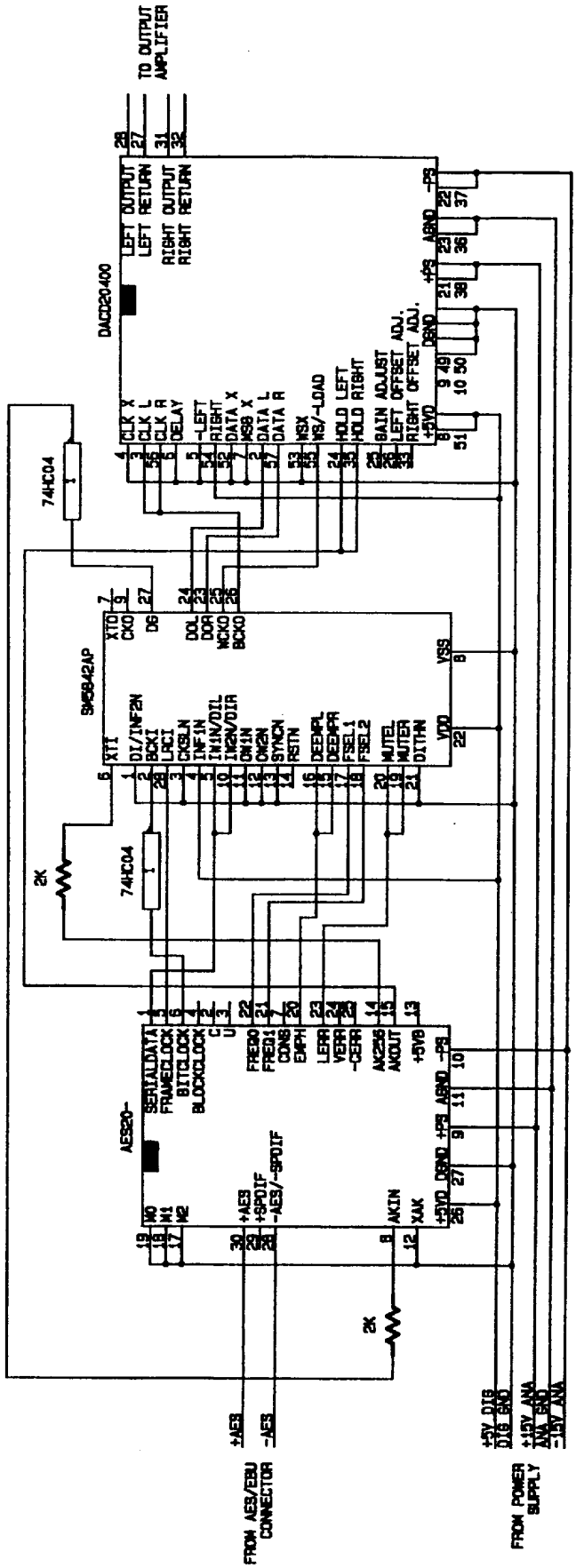

Fig. 12 AES20 USED WITH SM5842 AND DAC020400

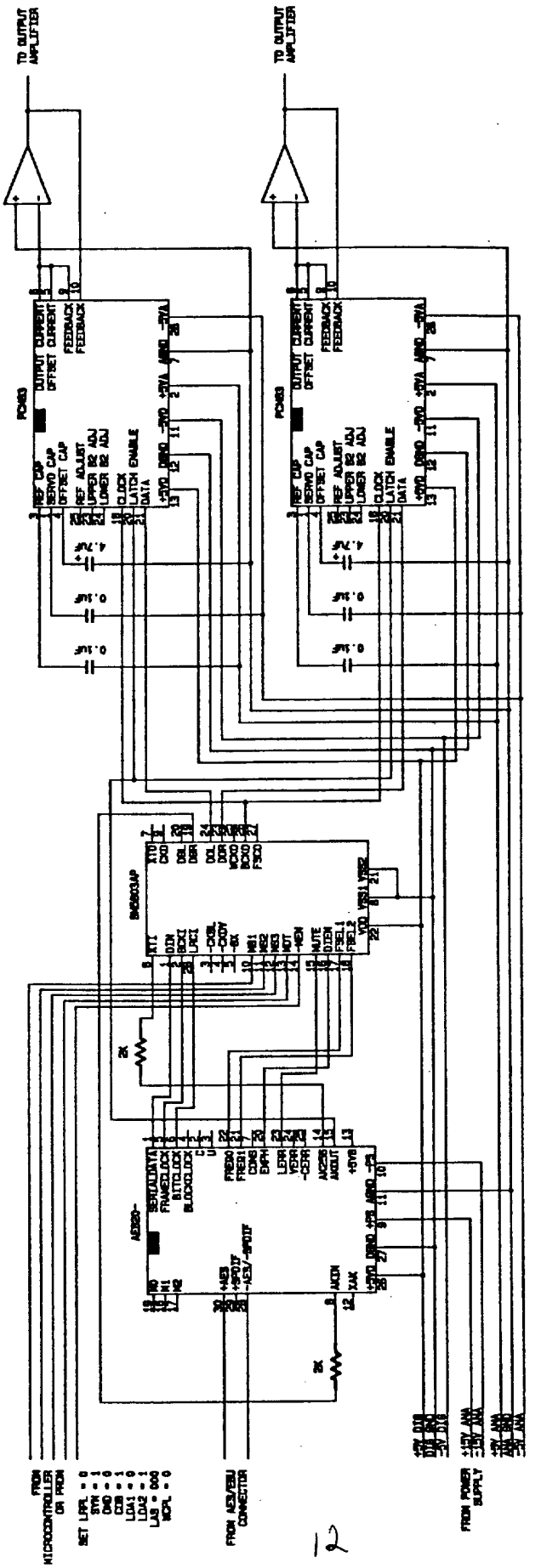

Fig. 13 AES20 USED WITH BB3603 AND PCM63

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